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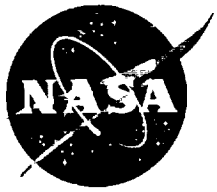

Integrated Circuit Electromagnetic Immunity Handbook

J.G. Sketoe
Boeing Information, Space and Defense Systems, Seattle, WA

Prepared for Marshall Space Flight Center
under Contract NAS8-98217
and sponsored by
The Space Environments and Effects Program
managed at the Marshall Space Flight Center

August 2000

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Abstract

This Handbook presents the results of the Boeing Company effort for NASA under contract NAS8-98217. Immunity level data for certain integrated circuit parts are discussed herein along with analytical techniques for applying the data to electronics systems. This handbook is built heavily on that produced in the seventies by McDonnell Douglas Astronautics Company (MDAC, MDC Report E1929 of 1 August 1978 entitled Integrated Circuit Electromagnetic Susceptibility Handbook known commonly as the ICES Handbook which has served countless systems designers for over 20 years.

Sections 2 and 3 supplement the device susceptibility data presented in Section 4 by presenting information on related material required to use the IC susceptibility information. Section 2 concerns itself with electromagnetic susceptibility analysis and serves as a guide in using the information contained in the rest of the handbook. A suggested system hardening approach is outlined, and an example of determining system-hardening requirements is presented in this chapter. Section 3 briefly discusses coupling and shielding considerations. For conservatism and simplicity, a worst case approach is advocated to determine the maximum amount of RF power picked up from a given field.

This handbook expands the scope of the immunity data in this Handbook is to of 10 MHz to 10 GHz. However, the analytical techniques provided are applicable to much higher frequencies as well. It is expected however, that the upper frequency limit of concern is near 10 GHz. This is due to two factors; the pickup of microwave energy on system cables and wiring falls off as the square of the wavelength, and component response falls off at a rapid rate due to the effects of parasitic shunt paths for the RF energy. It should be noted also that the pickup on wires and cables does not approach infinity as the frequency decreases (as would be expected by extrapolating the square law dependence of the high frequency roll-off to lower frequencies) but levels off due to mismatch effects.

1. INTRODUCTION

This Handbook presents the results of the Boeing Company effort for NASA under contract NAS8-98217. Immunity level data for selected integrated circuit parts are presented along with analytical techniques for applying the data to electronics systems.

1.1 Background

In the decade of the seventies the U. S. Naval Surface Weapons Center - Dahlgren Laboratory was tasked to provide electromagnetic compatibility guidance for designers of electronic systems that must operate in high power electromagnetic environments. McDonnell Douglas Astronautics Company (MDAC), under contract to the U. S. Naval Surface Weapons Center - Dahlgren, developed a technology base of integrated circuits and discrete semiconductor susceptibility to microwave signals. MDC Report E1929 of 1 August 1978 entitled Integrated Circuit Electromagnetic Susceptibility Handbook (more commonly known as the ICES Handbook) documented the results. The ICES Handbook has been invaluable to countless systems designers for over 20 years.

However, advances in integrated circuit technology have drastically altered circuits design and performance characteristics. These changes have probably invalidated much of the earlier data. Therefore NASA has sponsored this present effort to provide updated circuit susceptibility data at an affordable cost. Test data was derived and is presented herein for use as fundamental design data for systems engineers.

1.2 Purpose

This handbook is intended to contain much of the information needed to estimate the RF immunity level of circuits that contain IC's, and to approach the hardening task required to ensure that these circuits will operate in high power RF environments. Chapters 2 and 3 supplement the device susceptibility data presented in Chapter 4 by presenting information on related material required to use the IC susceptibility information. Chapter 2 is concerned with electromagnetic susceptibility analysis and serves as a guide in using the information contained in the rest of the handbook. A suggested system hardening approach is outlined, and an example of determining system-hardening requirements is presented in this chapter. Chapter 3 briefly discusses coupling and shielding considerations. For conservatism and simplicity, a worst case approach is advocated to determine the maximum amount of RF power picked up from a given field.

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1.3 Test System Summary

As indicated in Figure 1-1, the Test System is computer controlled through the GPIB bus. The instrumentation responds in accordance with the flow chart. The computer commands the HP 83732B Signal Generator to generate a calibrated EMI signal of a specified frequency and amplitude. The computer software compensates for the calibrated losses (primarily the bias tee) within the test setup.

The EMI Input Switch, a 1x20 switch, couples the EMI signal to the pin under test via Bias Tees. The computer software then couples the EMI signal to the appropriate pin in turn as the test progresses. The Bias Tees are individually calibrated such that the computer compensates the Signal Generator output for the Bias Tee loss at the frequency of interest. And the computer adjusts for the proper power level based on the serial numbered bias tee by measuring the amplifier output level.

The HP 34970A Switch Controller is equipped with two modules: the HP 34901A Data Acquisition module, which measures the responses, and the HP 34903A switch which provides the bias and supply voltages (including zero or ground) to the chip. There is no reason to think the performance of a 7400 NAND gate would be the same in the four possible bias conditions, i.e., 00, 01, 10, and 11. Therefore, testing was done all possible combinations.

When commanded to measure, the HP 34901A measures all twenty channels. This results in an array that is processed by the S/W and compared with various thresholds to assess the IC's EMI Immunity level.

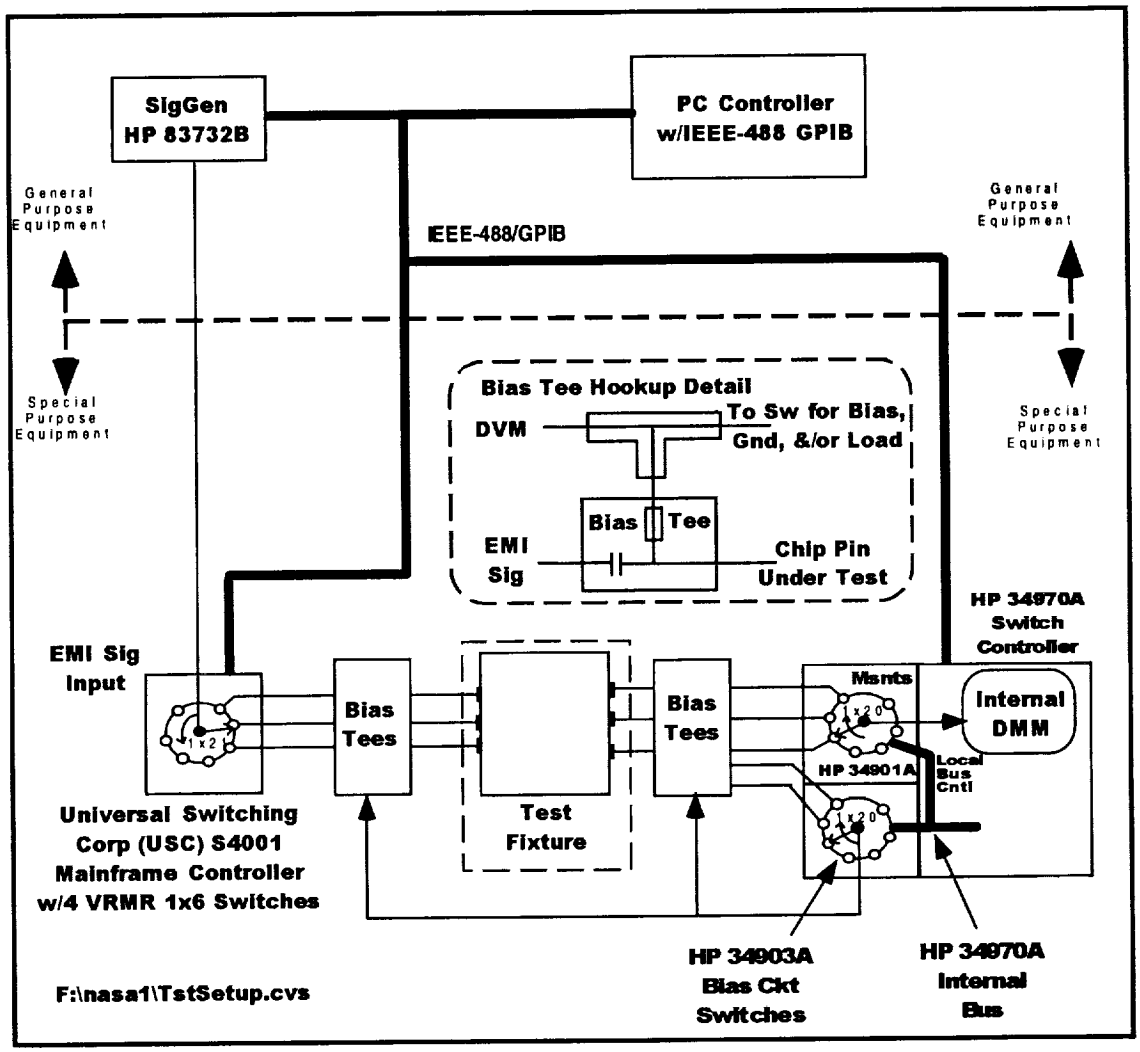


Figure 1-1. Test System

2. ELECTROMAGNETIC SUSCEPTIBILITY ANALYSIS

The material in this chapter is intended to aid system designers and EMC engineers in using the information presented later in this handbook in developing electronic systems capable of operating in high power RF environments. The basic situation of interest throughout this chapter is illustrated in Figure 2-1.

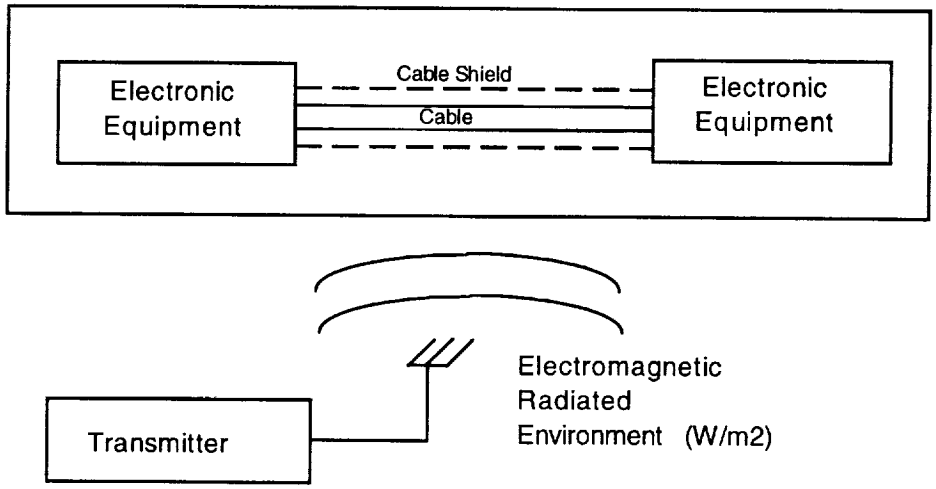


Figure 2.1. Basic Situation of Interest.

A system consisting of several electronic "black boxes" with interconnecting cables is contained within a system outer enclosure (skin). Electromagnetic radiation incident upon the system outer enclosure couples through apertures into the system interior. The internal EM fields induce RF voltage on the system interconnecting cables, which conduct them into the electronic "black boxes, where semiconductor devices such as integrated circuits are located. The RF voltage can be rectified by the semiconductor devices, and offset voltage and currents may be produced that are large enough to upset the operation of the electronic circuits.

To ensure electromagnetic compatibility of electronic systems and to reduce the development time and cost of such systems, it is suggested that a well-organized hardening design plan be used. Section 1 of this chapter presents a proposed system hardening procedure to be used by system designers and EMC engineers to ensure that electronic systems will function in a given EM environment. Section 2 describes a method of determining system-hardening requirements from the EM environment specifications and from information on pickup and component susceptibility. This procedure indicates how much

additional hardening is required through such methods as shielding, filtering, etc., for the system to meet the given environment specifications.

2.1 System EMV Hardening Approach

Figure 2.2 illustrates a proposed step-by-step system hardening task flow to ensure compatibility of electronic systems with a specified EM environment at a minimum of development time and cost. The electromagnetic environment must be known as the first step of the hardening task flow. The environment is dictated in terms of the frequencies and power densities that the system will encounter during its lifetime, including both operational and non-operational periods. Usually, the customer furnishes the environment specification to the system designer. If this is not the case, electromagnetic environment data is available in MIL-HDBK-235, or measurements or analysis of the actual environment may have to be made.

Next the pickup levels and component immune levels determined as two independent tasks. The chapter on coupling and shielding (Chapter 3) gives information on determining cable pickup from environmental power density values. A worst case approach is recommended, where the maximum pickup levels by the system cables are determined. The component immunity chapter (Chapter 4) provides information on the minimum (worst case) power levels that cause upset in integrated circuits.

Once the pickup levels and component susceptibilities are determined, a worst case vulnerability assessment can be performed. Comparing the expected maximum pickup level to the minimum power level that will cause component interference does this. The hardening requirement is the ratio of the maximum expected pickup level to the minimum component susceptibility level. An example of the determination of the hardening requirement is given in the next section.

Several courses of action are available to the system designer, depending on the hardening requirement determined in the previous step. If the hardening requirement is less than 0 dB, no hardening is needed and time and cost can be saved by simply proceeding to the final system test. If, however, hardening is required (indicated by a hardening requirement value greater than 0 dB), two paths are available to the system designer. If the required hardening is less than 30 dB, the most effective method is probably to proceed with the detailed

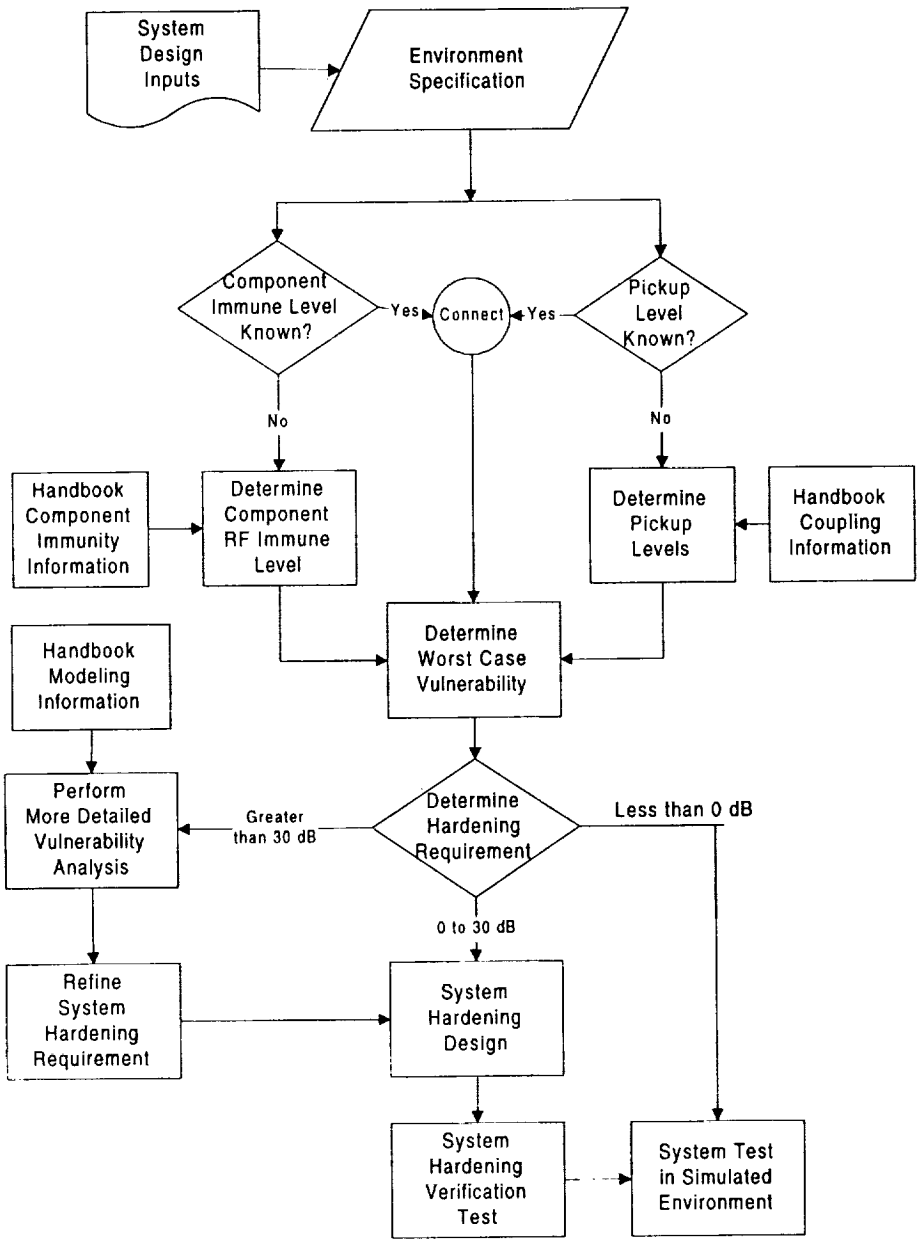


Figure 2-2. System Hardening Task Flow

hardening design. Thirty dB is a somewhat arbitrary figure. It represents a readily attainable hardening value, so that additional analysis is probably not needed. If, however, the hardening requirement is greater than 30 dB, a more detailed vulnerability analysis is probably worthwhile. This may include reassessment of the assumptions made in determining worst case vulnerability

and a reassessment of the use of worst case component susceptibility data. The designer may wish to consider several interference reduction options, including screening for less susceptible components and the use of less susceptible circuit designs. At this point the designer may isolate those portions of the system requiring more protection by placing them in separate enclosures, so that hardening efforts can be concentrated in these areas, saving cost, time, and weight in obtaining the required system protection.

The system hardening design involves the choice of appropriate filters, gaskets, shielded cables, connectors, lossy materials, enclosures, etc. The hardening design also involves the integration of all of these components into the system. Tests should be performed to validate the hardening design. If possible, these should be performed so that individual hardening approaches are verified separately. For example, the shielding effectiveness of the outer enclosure can be measured without the system circuitry installed. An iterative method may be used where the hardening approach is tested to evaluate whether additional hardening is needed. If so, the hardening is added and the test repeated. After implementation of all of the individual hardening approaches, a test of the completed system should be made to verify the effectiveness of the hardening techniques. The final step in the hardening task flow is a system test in a simulated environment to ensure that the EMV specifications are met. The customer may specify the details of the final system test.

2.2 Determination of System Hardening Requirements

This section contains an example of how to calculate hardening requirements for electronic systems. Electromagnetic environment levels (in terms of power density) are determined according to the stockpile to end-of-service life cycle of the systems of interest, and a table or graph of required test levels is usually included in contractual documents. The amount of power an unshielded wire or cable will pick up from this environment depends on such variables as frequency, aspect angle, terminating impedance, etc. One method for determining the maximum amount an unshielded wire will pick up is given by the formula (from Chapter 3):

$$P = 0.13\lambda^2 P_d$$

where P is the maximum pickup power (watts), λ is the wavelength (meters) of interest, and P_d is the power density (Watts/meter^2). Experimental data supports the use of this relationship for frequencies greater than 100 MHz.

Using this formula, the maximum amount of power expected on system wiring can be calculated from the environment level. The resulting pickup power levels are illustrated in Figure 2-3.

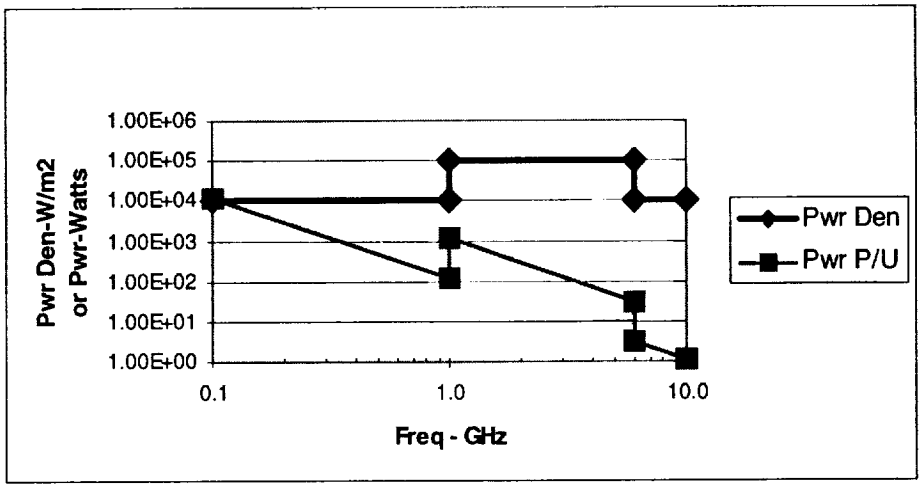


Figure 2-3 Sample Calculation of Pickup Power From Given Power Density

3. COUPLING AND SHIELDING CONSIDERATIONS

This chapter briefly presents the rationale and methods for estimating worst case RFI pickup on system cables and wires for use in estimating system hardening requirements by comparison to the IC susceptibility data. The problem is divided into two parts: estimating pickup on "unshielded" cables, and accounting for inherent shielding produced by system structure, proximity of other cables, etc.

3.1 RFI Pickup on Unshielded Wires

The approach used here is to consider the interconnect wires attached to semiconductor component terminals (perhaps by way of printed circuit conductors, connectors, etc.) as generalized antennas, i. e., energy transducers which convert the radiated RF energy to conducted quantities of RF voltage and current. Predicting exact results is an immensely complicated task for all but the simplest geometry's and load conditions so that a more tractable, but less precise, technique is needed.

It can be observed that the amount of power delivered to a load which terminates a typical electronic system interconnect cable in a prescribed EM field will vary greatly with changes in frequency, terminating load, and geometrical factors (including wire routing and aspect angle relative to interfering source). Figure 3-1 illustrates the manner in which pickup on a typical wiring specimen varies with aspect angle (the figure shows a reconstruction of the three-dimensional pickup pattern as determined by different planar "slices"). Since little or no control of the relative orientation between the interference source and victim wire bundle is available anyway, considering the aspect angle as a random variable and treatment of the pickup as a probabilistic function of the aspect angle is useful.

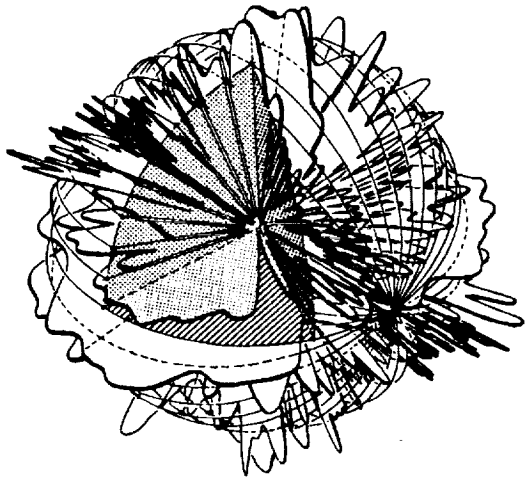


Figure 3-1. Three Dimensional Representation of Wire Pickup Pattern

Numerous measurements on representative cables have shown that the power picked up in planar fields can be described by a log-normal relationship (i. e., the power measured in logarithmic units such as dBm is distributed normally) with a standard deviation between 3 and 6 dB. See Figure 3-2. Measurements using different length cables and different load impedance indicate that the measured distribution is relatively independent of such parameters (at least over the frequency range of 100 MHz to 10 GHz). Apparently, the only significant parameter is frequency (excluding shielding effects, which are discussed below).

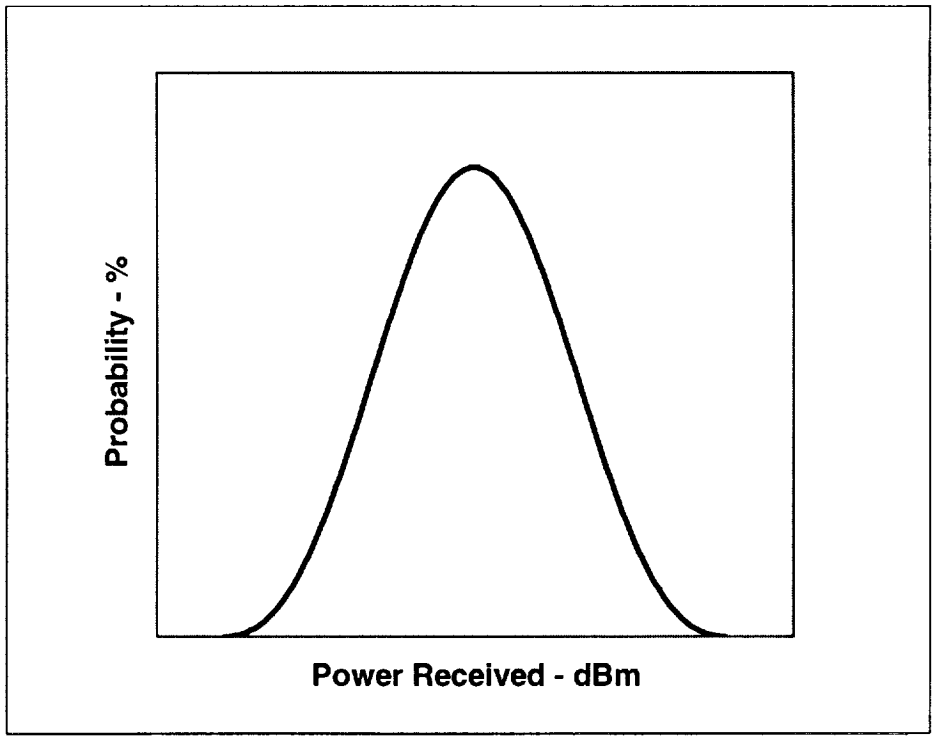


Figure 3-2. Typical Probability Density Function for Wire Pickup Pattern.

The frequency dependence is best considered from the worst-case point of view, i. e., maximum expected pickup versus frequency. To normalize results with respect to field quantities effective aperture is used to describe the wire pickup mechanism.

Thus the measured pickup power (in watts) is divided by the incident power density (in watts per square meter) to yield effective aperture (measured in square meters). Figure 3-3 shows measured maximum effective aperture for various wire lengths, loads, and frequencies. A least square fit to the log-log plot reveals that a frequency dependence very close to inverse square results and a constrained to fit (f^{-2}) is shown superimposed in the plot. Also shown is the standard error range and the theoretical curve for a matched, half-wave dipole (effective aperture = $0.13\lambda^2$). It is clear that using the simple expression for the half-wave dipole is reasonable upper bound for this experimental data.

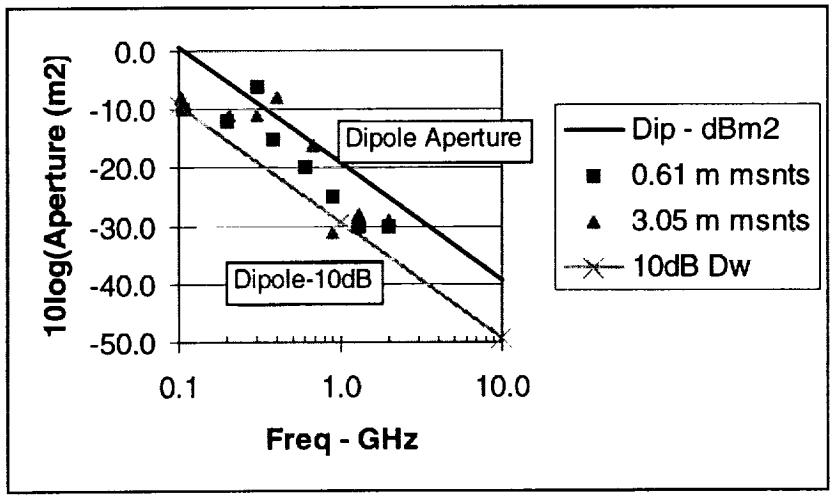


Figure 3-3. Measured Maximum Effective Apertures (A_e) of Various Wire Lengths

There are two difficulties with using the half-wave dipole expression that must be borne in mind. The first is that wires can be made to exhibit greater effective apertures than given by the half-wave dipole expression due to specific design and/or fortuitous focusing effects by system structure. For example, consider the increased pickup on a short dipole possible when a large parabolic reflector is properly located nearby. Most system configurations are not expected to produce such enhancement effects, however, so it seems unreasonable to do a worst-case system hardening design based upon such possibilities. Such possibilities strengthen the rationale for thoroughly checking system-hardening design in simulated environments.

The second difficulty with using the half-wave dipole expression comes when it is desired to extrapolate the function to lower frequencies where the inverse square frequency dependence leads to enormous effective apertures, which are not observed in practice. The paradox can be resolved by recalling that the half-wave dipole expression is for a matched half-wave dipole. The equivalent (Thevenin) driving impedance of the dipole approaches zero as the frequency approaches zero so that, for a particular load on a cable, the mismatch losses counter the increasing aperture effects and the load will receive a constant amount of power, in accordance with common experience.

In summary, use of the halfwave dipole relation for effective aperture estimates in the 100 MHz to 10 GHz range is recommended as a worst cast estimate of pickup in a radiated field environments. But the caveats about the probabilistic nature of the phenomena and possible focusing effects are also emphasized.

3.2 Shielding Effectiveness

The basic concept of an electromagnetic shield to be considered here is "something" that reduces the pickup on wires. Since the pickup on wires is a probabilistic function, the concept of shielding effectiveness must be consonant with the probabilistic description of pickup phenomena. The effects of "doing something to reduce the pickup on a wire" (i. e., "shielding" the wire) can be assessed in a manner similar to that used for "unshielded" wires. Figure 3-4 illustrates this by showing two pickup patterns (only one azimuth plane) superimposed. In general the effect of the "shield" is to reduce the pickup on the shielded wire and quantitative description of "how much" can be derived by comparing the two probability density functions as in Figure 3-5. Experience shows the shape of the "shielded" distribution is very similar to that of the "unshielded" distribution (although this is not true for strong focusing effects which invalidate the halfwave dipole assumption) so that the difference in mean pickup and the difference in peak pickup are the same.

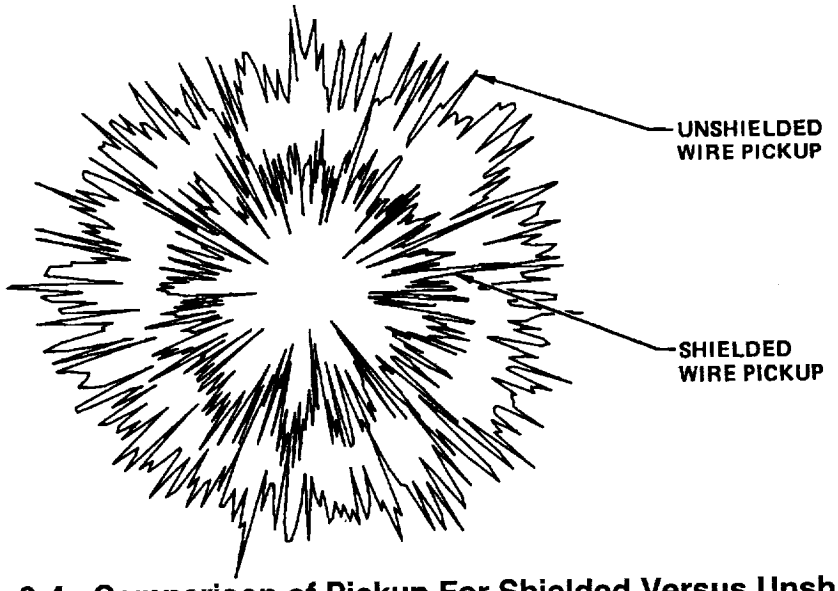


Figure 3-4. Comparison of Pickup For Shielded Versus Unshielded Wires

Figure 3-3 also reveals a potential trouble spot relative to the techniques used to measure the difference in pickup between a reference sample and test sample. In particular, note that it is possible to measure a larger pickup on the "shielded" sample than the "unshielded" sample. The area of the overlap in the two probability densities gives the probability of observing this condition and, unless the curves are widely separated, this probability may be significant. The most reliable technique for assessing shielding effectiveness (short of completely determining the probability density functions) is to measure the peak pickup for each configuration. MIL-STD-1377 (Navy) offers an efficient technique for accomplishing this goal over the frequency range of its applicability (generally greater than 100 MHz depending upon test chamber size).

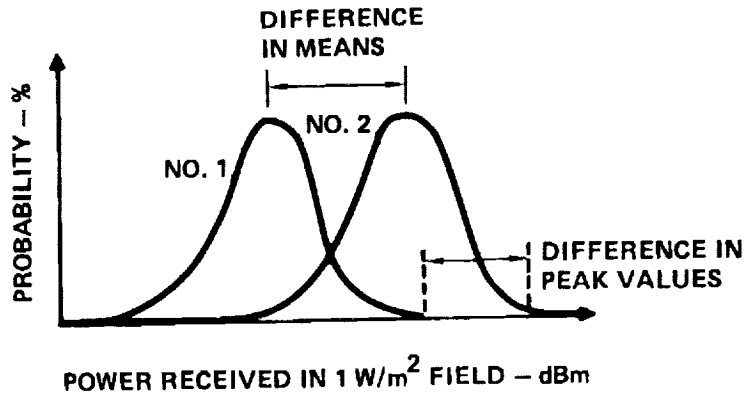


Figure 3-5. Probability Density Functions for Shielded and Unshielded Wires

4. COMPONENT SUSCEPTIBILITY

Charts 1 through 11 provided below are included herein for ready reference. They depict the immunity of the chips tested in this study. The EMI signal was generated by a calibrated source limited to +30 dBm (one watt). With the bias tee and line losses the equipment limitation was about 27 dBm. Consequently the Chart 1-11 near level plots at 27 dBm represent equipment limitations, not thresholds. The data presented represents the worst case of all measurements taken on a series of parts of a selected part number.

The data depict the immunity level to the first threshold by a solid line and the second threshold by a dashed line. On this TTL data from a starting Low (<0.4 volts) the first threshold was 0.8 volts output (below which the following circuit would interpret as a Low), and the second threshold was 2.0 volts (above which the following circuit would interpret as a High). In between (i.e., 0.8 to 2.0 volts) is undefined. Should the particular configuration under test begin with a High (>2.5 volts) the first threshold was 2.0 volts and the second was 0.8 volts. These values were taken from the manufacturer's specification for the parts tested.

Examination of Charts 1 through 10 indicates, in general, the immune level of TTL type devices appears to exceed 10 dBm for totem-pole devices. The open collector devices, 7405 and 74LS05, are slightly less immune (i.e., more susceptible) than their totem pole counterparts.

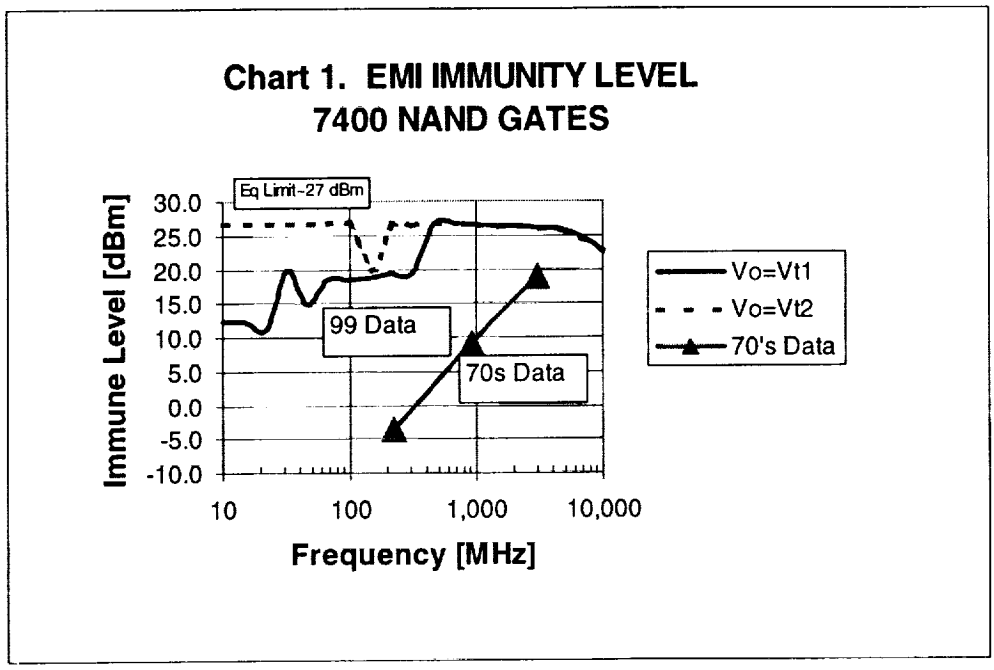


Chart 1. EMI IMMUNITY LEVEL
7400 NAND GATES
Eq Limit-27 dBm
99 Data
70s Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

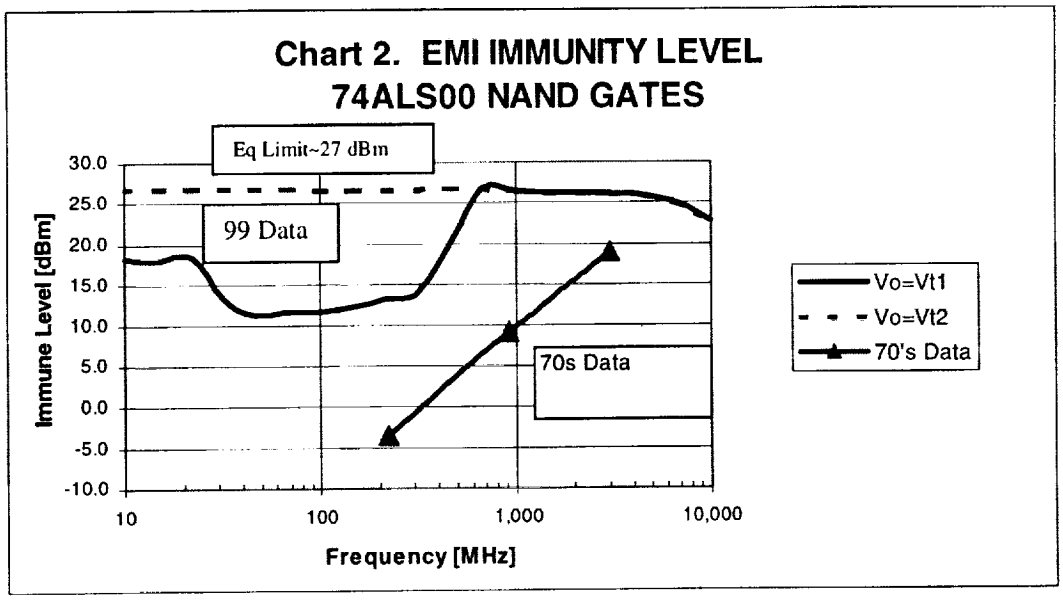


Chart 2. EMI IMMUNITY LEVEL
74ALS00 NAND GATES
Eq Limit-27 dBm
99 Data
70s Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

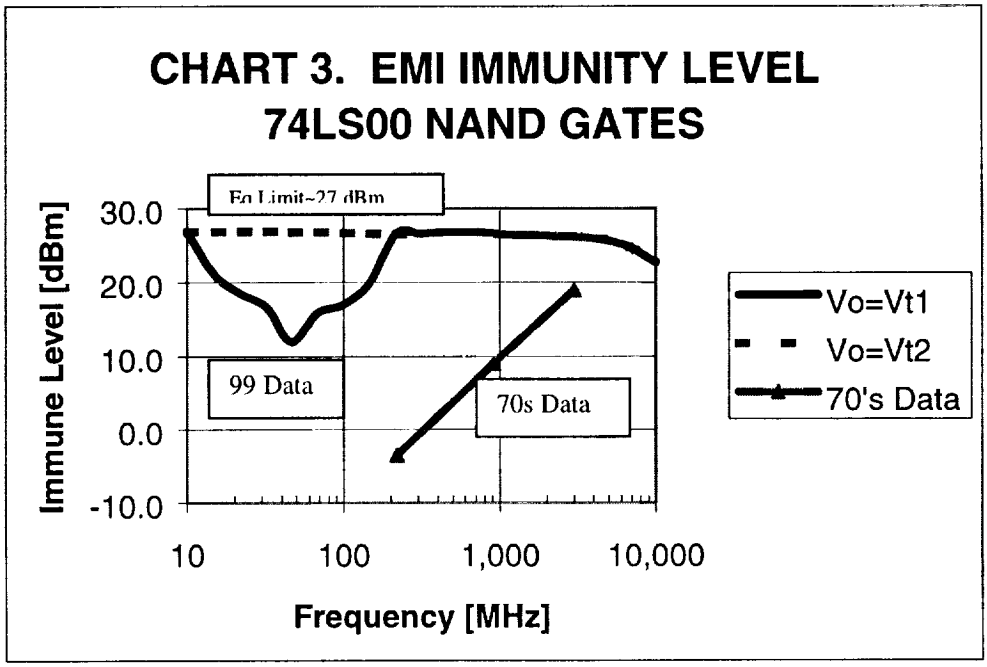


CHART 3. EMI IMMUNITY LEVEL
74LS00 NAND GATES
Eq Limit~27 dBm
30.0
20.0
10.0
0.0
-10.0
Immune Level [dBm]
99 Data
70s Data
Vo=Vt1
Vo=Vt2
70's Data
10
100
1,000
10,000
Frequency [MHz]

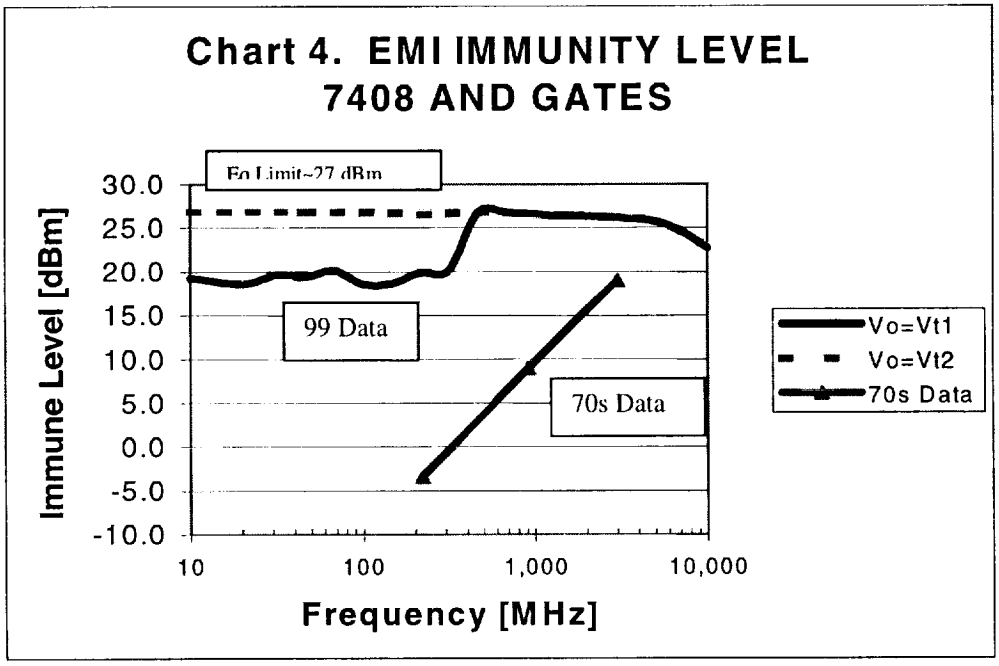


Chart 4. EMI IMMUNITY LEVEL
7408 AND GATES
Eq Limit~27 dBm
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
Immune Level [dBm]
99 Data
70s Data
Vo=Vt1
Vo=Vt2
70s Data
10
100
1,000
10,000
Frequency [MHz]

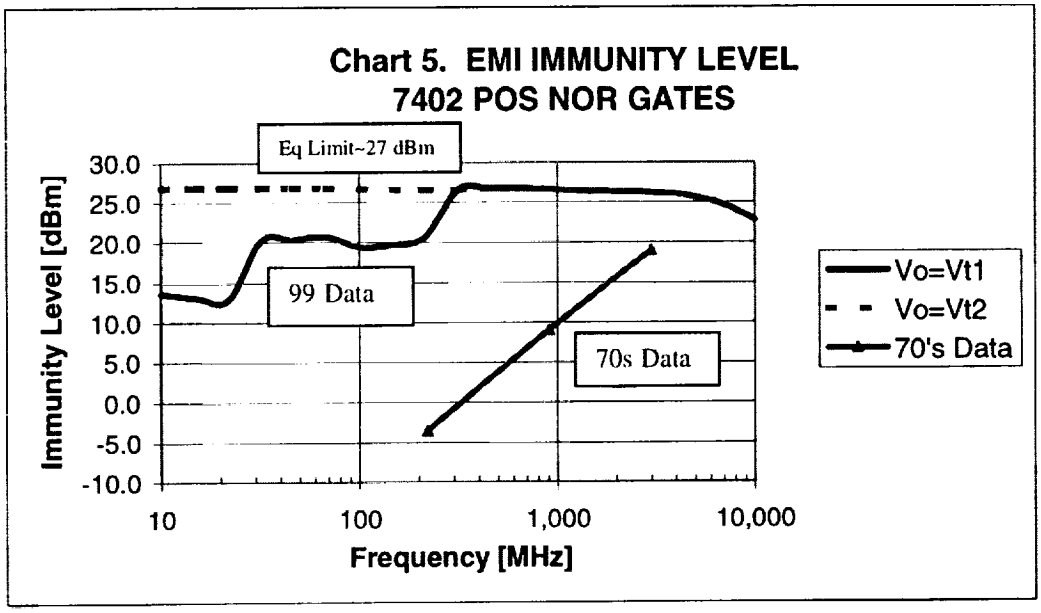


Chart 5. EMI IMMUNITY LEVEL
7402 POS NOR GATES
Eq Limit~27 dBm
99 Data
70s Data
Immunity Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

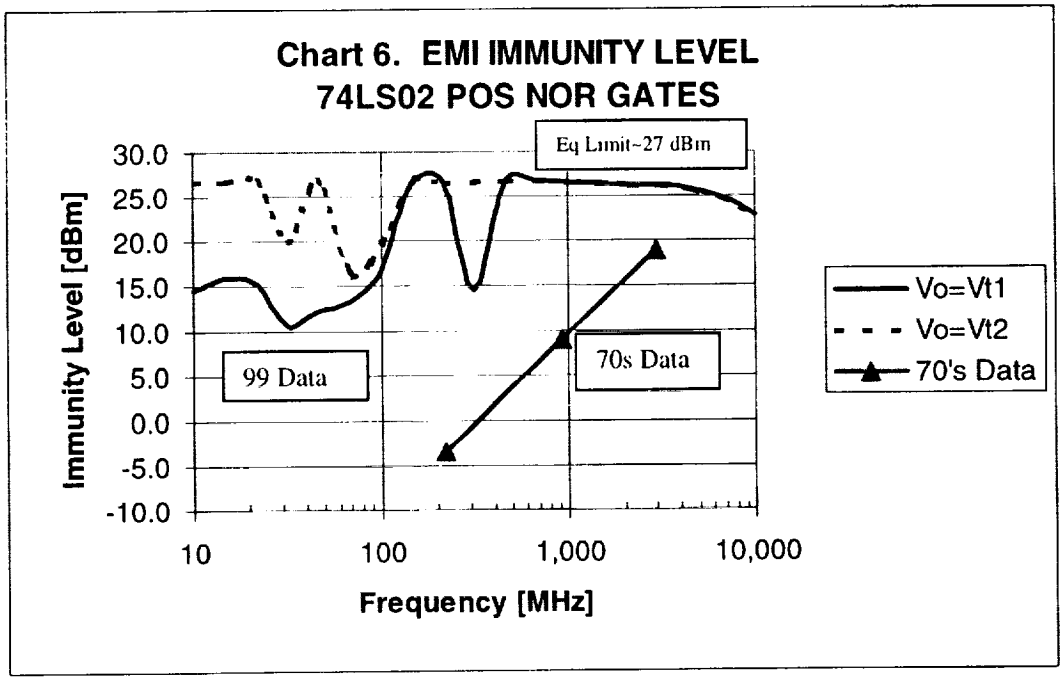


Chart 6. EMI IMMUNITY LEVEL
74LS02 POS NOR GATES
Eq Limit~27 dBm
99 Data
70s Data
Immunity Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

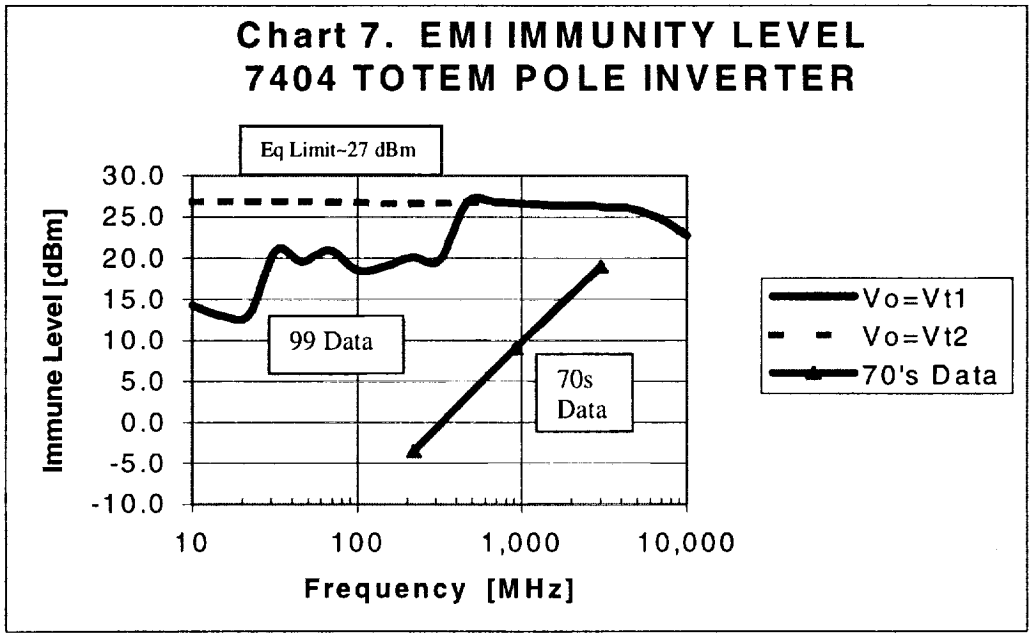


Chart 7. EMI IMMUNITY LEVEL
7404 TOTEM POLE INVERTER
Eq Limit-27 dBm
99 Data
70s Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

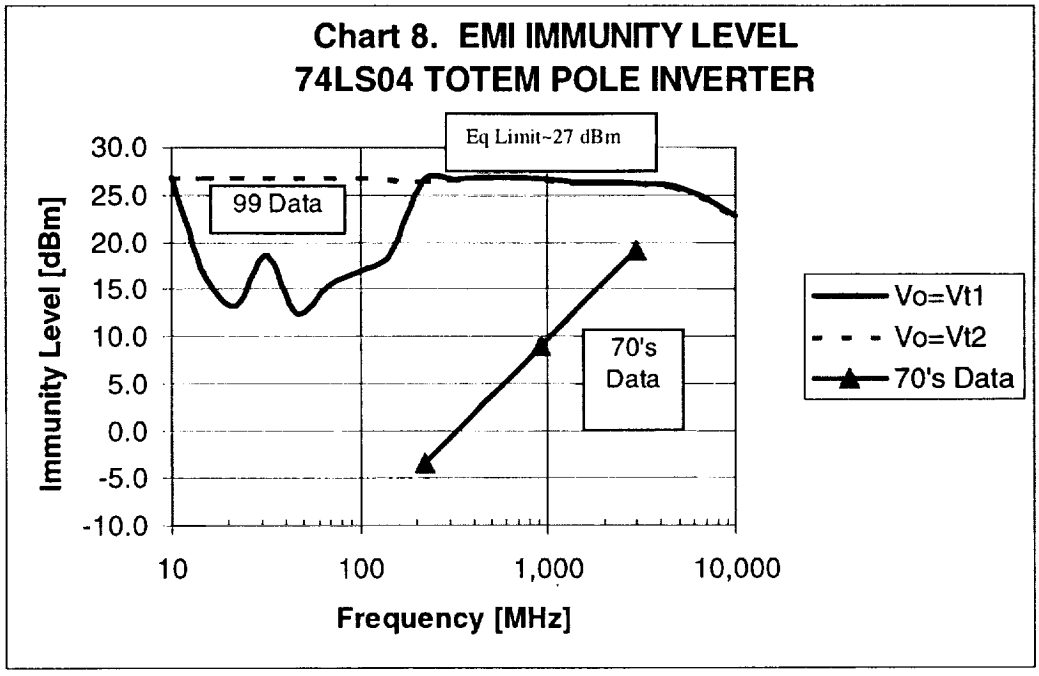


Chart 8. EMI IMMUNITY LEVEL
74LS04 TOTEM POLE INVERTER
Eq Limit-27 dBm
99 Data
70's Data
Immunity Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

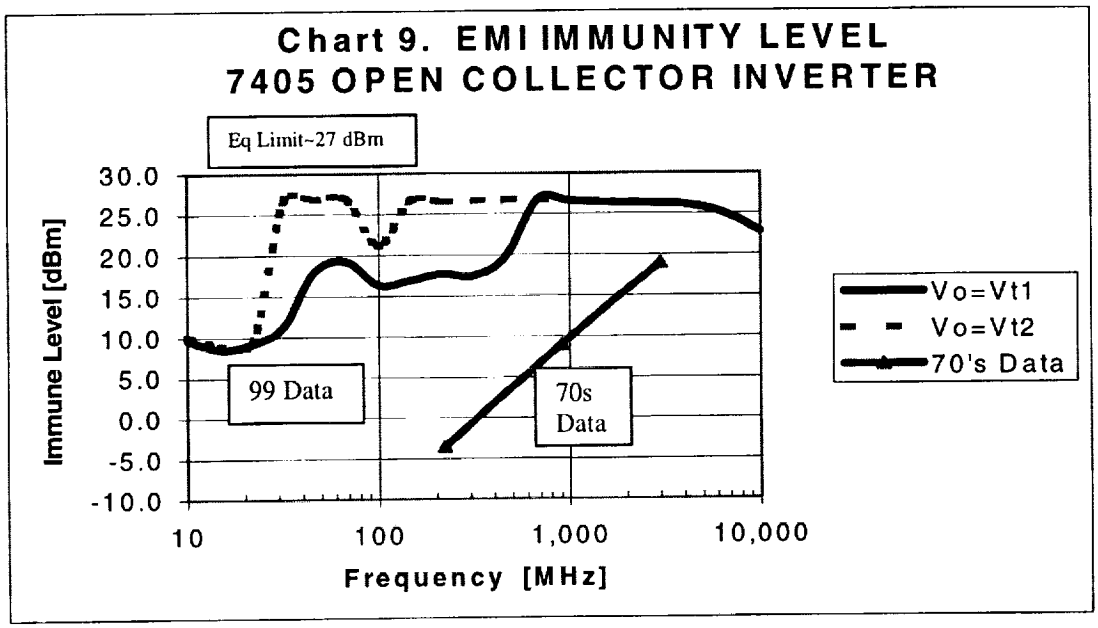


Chart 9. EMI IMMUNITY LEVEL
7405 OPEN COLLECTOR INVERTER
Eq Limit-27 dBm
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
Immune Level [dBm]
99 Data
70s Data
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

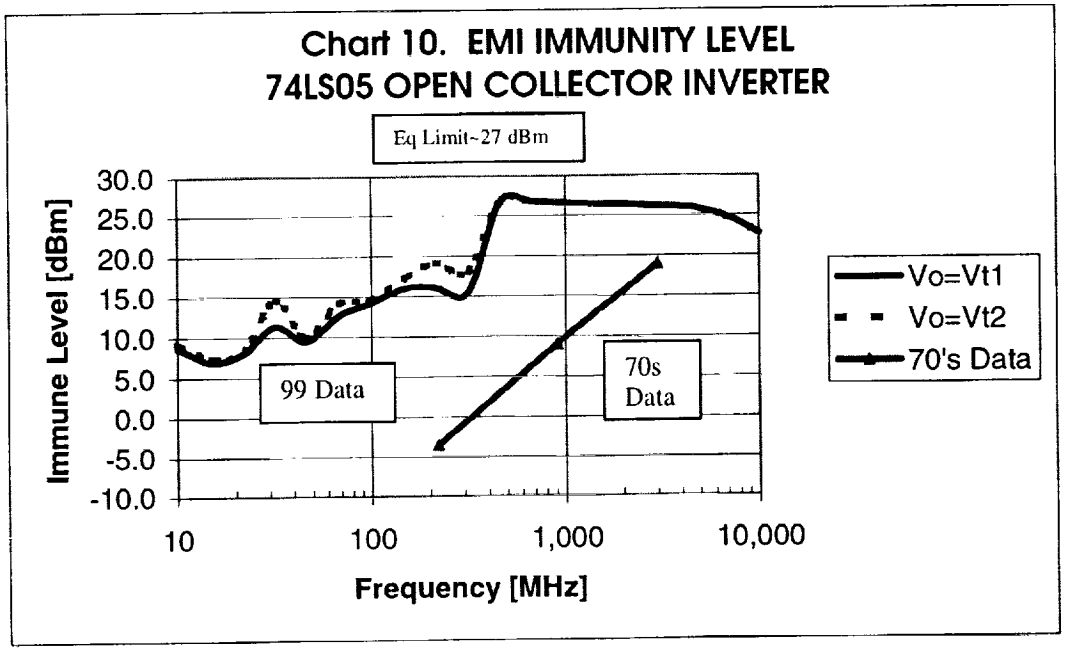


Chart 10. EMI IMMUNITY LEVEL
74LS05 OPEN COLLECTOR INVERTER
Eq Limit-27 dBm
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
Immune Level [dBm]
99 Data
70s Data
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

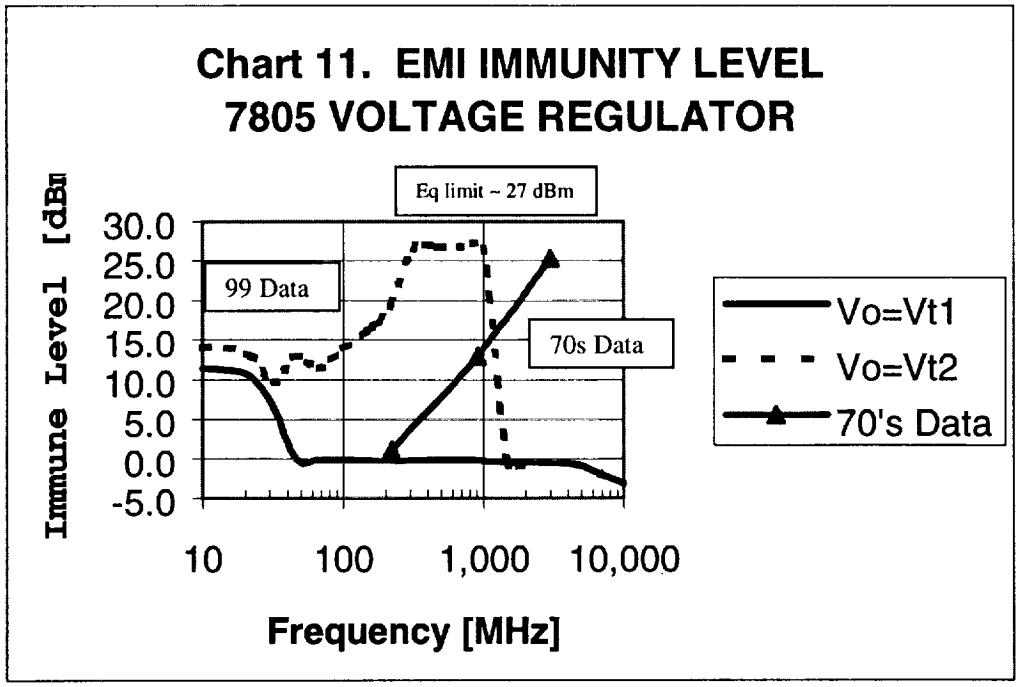


Chart 11. EMI IMMUNITY LEVEL
7805 VOLTAGE REGULATOR
Eq limit ~ 27 dBm
99 Data
70s Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

References

1. Integrated Circuit Electromagnetic Susceptibility Handbook, McDonnell Douglas Corporation Report MDC E1929, 1 August 1978

2. Report No. D950-10465-1 — Integrated Circuit Electromagnetic Immunity, Volume 1 — Final Report, 31 December 1999

3. Report No. D950-10465-2 — Integrated Circuit Electromagnetic Immunity Volume 2 — Handbook, 31 December 1999

4. Report No. D950-10466-1 — Integrated Circuit Electromagnetic Immunity User's Manual, 31 December 1999

Appendix

Excerpt from

"Integrated Circuit Electromagnetic Immunity, Volume 1 - Final Report"

Additional information on the Test System Description and Test Process.

Table of Contents

List of Figures

List of Charts

Abstract

This report documents the Boeing Company efforts to develop an automated test system for the determination of integrated circuit immunity to Radio Frequency Interference. Actual test data taken by the system was used both as a demonstration of the test system and as fundamental design data for systems engineers. A database containing this information is contained in electronic format as Boeing Document Number D950-10465-2. Engineering applications guidance is provided in Boeing Document Number D950-10466-1, Integrated Circuit Immunity Handbook. Detailed operating instructions are provided in Boeing Document Number D950-10467-1, Integrated Circuit Electromagnetic Immunity User's Manual.

In the decade of the seventies McDonnell Douglas Astronautics Company (MDAC), under contract to the U. S. Naval Surface Weapons Center - Dahlgren, developed a technology base of integrated circuits and discrete semiconductor susceptibility to microwave signals. MDC Report E1929 of 1 August 1978 entitled Integrated Circuit Electromagnetic Susceptibility Handbook (more commonly known as the ICES Handbook) documented the results. References herein to those results are labeled as "70s Data" to distinguish it from the data obtained under this contract identified as "99 Data." The ICES Handbook has been invaluable to countless system designers for over 20 years.

The advancement of integrated circuit technology has drastically altered circuits design and performance characteristics. As a result the behavior of today's parts differ substantially with those of yesteryear. NASA has sponsored this present effort to develop a technology to obtain and maintain updated integrated circuit immunity data at an affordable cost. For comparative purposes some of the seventies data is included.

A fully functional Integrated Circuit Test System has been developed with instrument capabilities that far exceed the capabilities available during the earlier work. Computer control of test equipment is much faster and more accurate. High-level instrument control languages, such as, LabVIEW have been used to speed software development. It is a computer controlled set of instruments, switches and connecting hardware for applying the desired operating voltages and RF interference signals while automatically reading and recording the response. The result is an improvement of orders of magnitude in the time required to perform such testing.

Details of the experimental test results and linear integrated circuits are presented in Section A3. There are interesting comparisons to be made between present technology performance and that of 25 years ago. Today's 7400 line of Integrated Circuits are significantly more tolerant of EMI than were those tested in the seventies. The 7400 NAND gate's immunity level increased over several dB.

The primary emphasis of this effort was the development of an automated test system and methodology. A need still exists to build a large database of parts susceptibility information. It is recommended that consideration be given to funding a production phase of this effort that concentrates on acquiring parts susceptibility data. Also, some meaningful improvements can be made in the LabView software control program to enhance the reliability and productivity of the test process along with further enhancement of automated statistical analyses of the resulting data.

Key Words

Conducted Susceptibility

Electromagnetic Compatibility

Electromagnetic Interference

EMC

EMI

IC

Immunity

Integrated Circuit

Lab View

Susceptibility

Test Fixture

TTL

A1. Introduction

This document presents the results of the Boeing Company effort for NASA under contract NAS8-98217. This effort was directed toward the development of an automated test system for the determination of integrated circuit immunity to Radio Frequency Interference. Also included was development of actual test data for use both as a demonstration of the test system and as fundamental design data for systems engineers. A database containing this information is contained in electronic format as Boeing Document Number D950-10465-2. The test results are reported herein along with engineering applications guidance in Boeing Document Number D950-10466-1, Integrated Circuit Immunity Handbook. Detailed operating instructions are provided in Boeing Document Number D950-10467-1, Integrated Circuit Electromagnetic Immunity User's Manual.

A1.1 Background

In the decade of the seventies the U. S. Naval Surface Weapons Center - Dahlgren Laboratory was tasked to provide electromagnetic compatibility guidance for designers of electronic systems that must operate in high power electromagnetic environments. McDonnell Douglas Astronautics Company (MDAC), under contract to the U. S. Naval Surface Weapons Center - Dahlgren, developed a technology base of integrated circuits and discrete semiconductor susceptibility to microwave signals. MDC Report E1929 of 1 August 1978 entitled Integrated Circuit Electromagnetic Susceptibility Handbook (more commonly known as the ICES Handbook) documented the results. References herein to those results are labeled as "70s Data" to distinguish it from the data obtained under this contract identified as "99 Data." The ICES Handbook has been invaluable to countless system designers for over 20 years.

A1.2 Purpose

The advancement of integrated circuit technology has drastically altered circuits design and performance characteristics. As a result today's parts behave differently than those of yesteryear; which probably invalidates much of the earlier data. NASA has sponsored this present effort to develop a technology to obtain updated integrated circuit immunity data at an affordable cost. The thrust has been the development of the semi-automated test system and method. The cost of the Navy sponsored program was in the millions of dollars. NASA is seeking a very significant cost gain through the use of greatly improved test instrumentation and computer control of testing and data handling. For comparative purposes some of the seventies data is included.

Present instrument capabilities far exceed the capabilities available during the earlier work. Computer control of test equipment is much faster and more

accurate. High-level instrument control languages, such as LabVIEW have been used to speed software development. The primary user interface is through the computer with LabView screens.

A fully functional Integrated Circuit Test System has been developed. It is described in Section A2. It is a computer controlled set of instruments, switches and connecting hardware for applying the desired operating voltages and RF interference signals while automatically reading and recording the response. The result is an improvement of orders of magnitude in the time required to perform such testing.

A1.3 Summary Of Test Results

Details of the experimental test results and linear integrated circuits are presented in Section A3. There are interesting comparisons to be made between present technology performance and that of 25 years ago. For example, today's 7400 line of Integrated Circuits appear to be significantly more tolerant of EMI than were those tested in the seventies. Consider a 7400 NAND gate biased with its output low, and an EMI signal injected on the output pin which represents the worst case tested to date. At 220 MHz, for older technology, 10 dBm was required to increase the output voltage error threshold to 0.8 volts. In today's testing over the range of 22 MHz to 300 MHz, an EMI signal of approximately 20 dBm was required to increase the output to 0.8 volts. Injecting higher power levels for higher thresholds yielded similar results. In the seventies at 60 mW (17.8 dBm) the output voltage exceeded 2.0 volts, a level at which logic errors are guaranteed. For the present testing activity over 10 MHz to 10 GHz the peak available power of 28-30 dBm would only cause an output of 1.7 volts, slightly below the upper threshold of 2.0 volts.

In general, linear circuits: are more sensitive to voltage offsets caused by RF energy than digital circuits, where logic states are defined in terms of voltage ranges. The interference effects generally decrease with increasing frequency of the interfering signal. As an example of interference in linear integrated circuits a three samples of 7805 voltage regulator were tested. The results are shown in Chart A11.

A1.4 Recommendations

The primary emphasis of this present effort has been the development of the automated test system and methodology. In the process, some very useful parts related data has been acquired, but the need still exists to build a large database of parts susceptibility information. It is recommended that consideration be given to funding a production phase of this effort that concentrates on acquiring parts susceptibility data. Also, some meaningful improvements can be made in the LabView software control program to enhance the reliability and productivity of the test process along with further enhancement of automated statistical analyses of the resulting data.

A2. System Description

The test system consists of the following instruments and equipment.

- HP 83732B Synthesized Signal Generator – 10 MHz-20 GHz
- HP 34970A Data Acquisition/Switch Unit (Voltmeter), with boards;
- HP 34901A 20-Channel Multiplexer Module
- HP 34903A 20-Channel Switch Module
- US (Universal Switching Corporation) Model 11284, DC-18GHz Microwave Switching System
- HP 6236B Triple Output Power Supply
- Test Fixture with Zero Insertion Force IC 20 pin socket and 20 connection cables with bias tees and insertion/measurement inputs.
- IBM P90 computer, equipped with National Instruments GPIB Card.

The test is controlled through the computer using National Instruments LabView software and the General Purpose Interface Bus (GPIB).

A2.1 Test System Description

As indicated in Figure A2-1, the Test System is computer controlled through the GPIB bus. The instrumentation responds in accordance with the flow chart Figure A3-3 discussed below. The computer commands the HP 83732B Signal Generator to generate a calibrated EMI signal of a specified frequency and amplitude. The computer software compensates for the calibrated losses (primarily the bias tees) within the test setup.

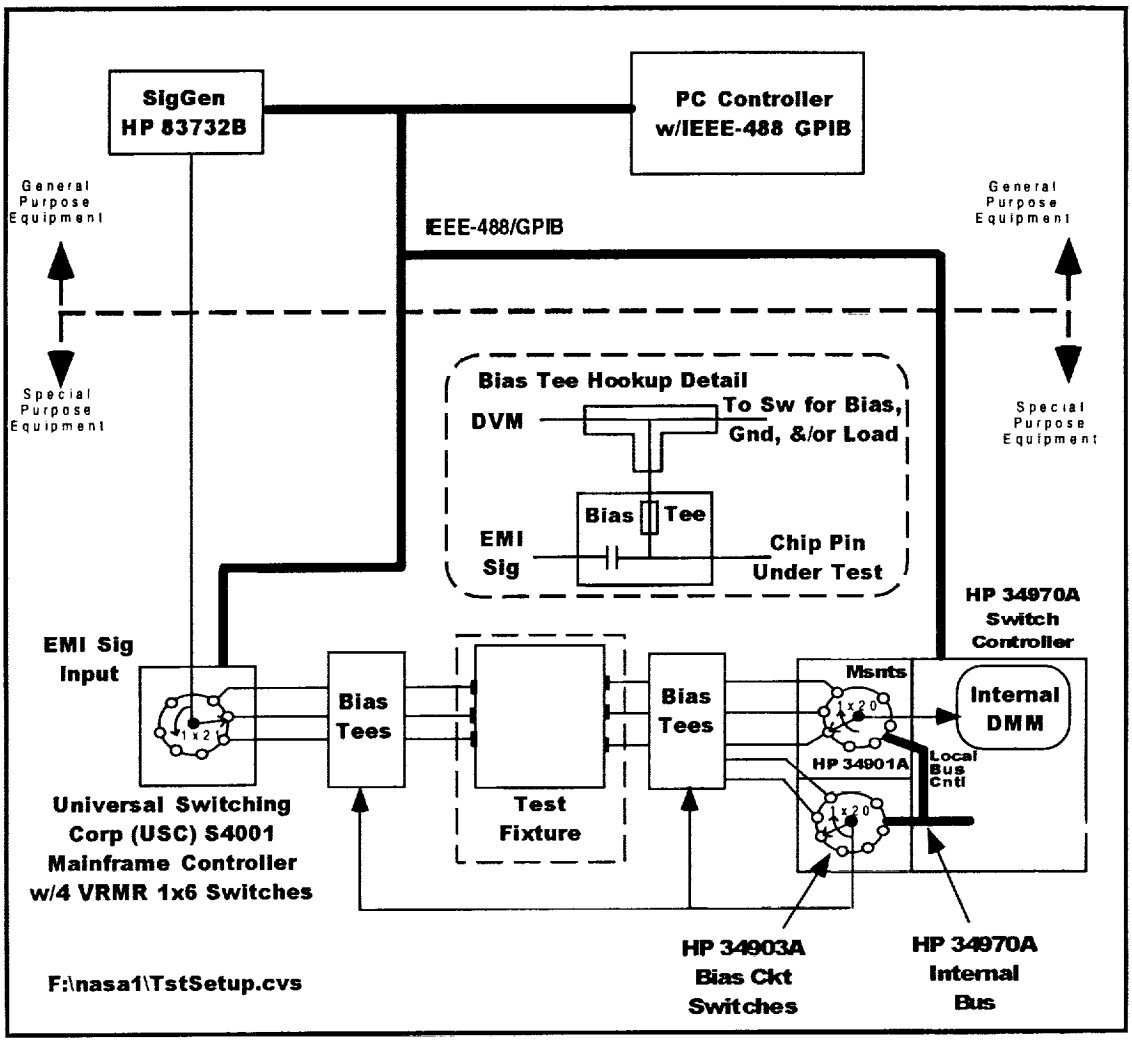


Figure A2- 1. Test system

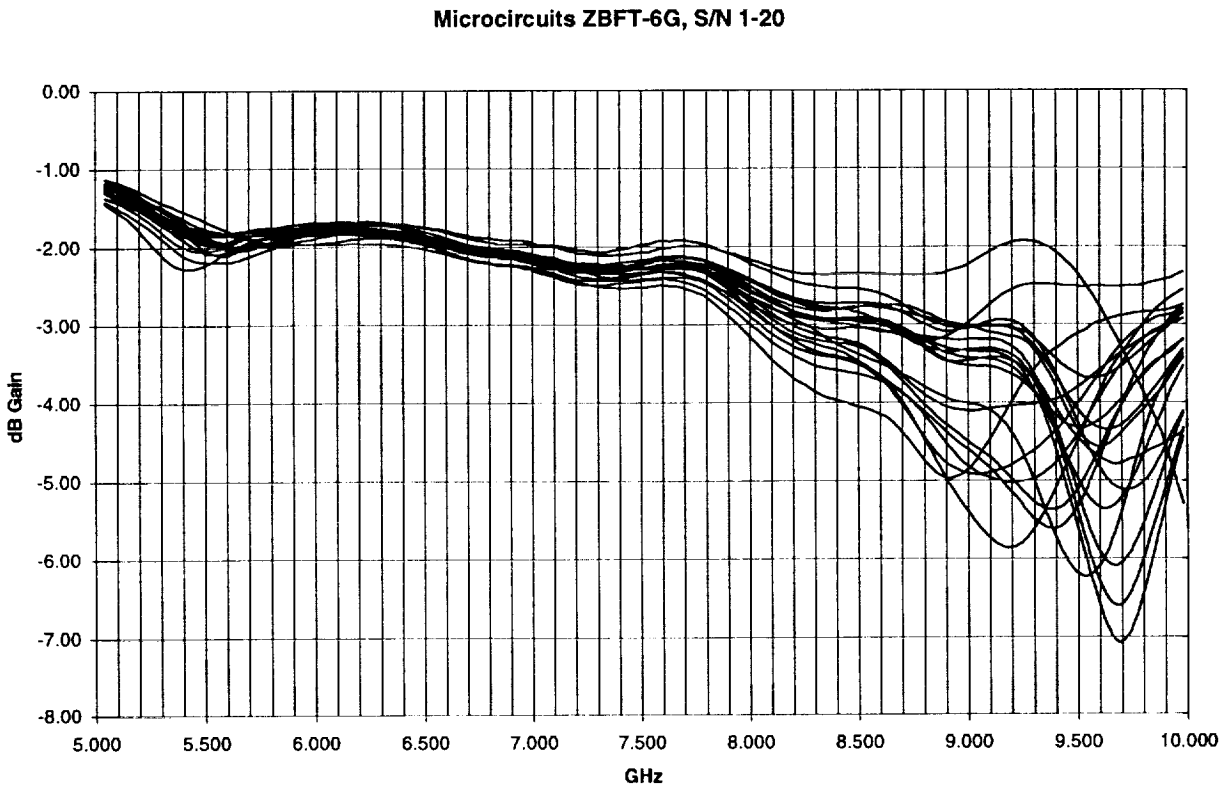
The EMI Input Switch, a 1x20 switch, couples the EMI signal to the pin under test via Bias Tees. The computer software then couples the EMI signal to the appropriate pin in turn as the test progresses. The Bias Tees are individually calibrated such that the computer compensates the Signal Generator output for the Bias Tee loss at the frequency of interest. And the computer adjusts for the proper power level based on the serial numbered bias tee.

The HP 34970A Switch Controller is equipped with two modules: the HP 34901A Data Acquisition module, which of course acquires the voltages, and the HP 34903A switch which provides the bias and supply voltages (including zero or ground) to the chip. There is no reason to think the performance of a 7400 NAND gate would be the same in the four possible bias conditions, i.e., 00, 01, 10, and 11. Therefore testing was done using all possible combinations.

When commanded to measure, the HP 34901A measures all twenty channels. This results in an array that is processed by the S/W and compared with various thresholds to assess the IC's EMI Immunity level.

A2.2 Bias Tee Calibration

While the Bias Tee manufacturer's specification stops at 6 GHz, the bias tees were individually calibrated for EMI signal loss from 10 MHz to 10 GHz. The resulting traces, plotted in Figure A2-2, indicate that with compensation, they are usable to



10 GHz.

Figure A2- 2. Calibration Curves, Minicircuits ZBFT-6G

2.3 Test Fixture

A cabled test fixture is shown in Figure A2-3. As depicted the fixture is equipped with the older bias tees from the seventies effort. The lightly colored coax is the EMI signal routing. The EMI signal goes through the arms of the bias tee directly into a short (12 inches) coax inside the fixture where it terminates into a PCB SMA connector. The PCB traces are controlled at 50 ohms and terminate on the pins of a 20-pin ZIF socket.

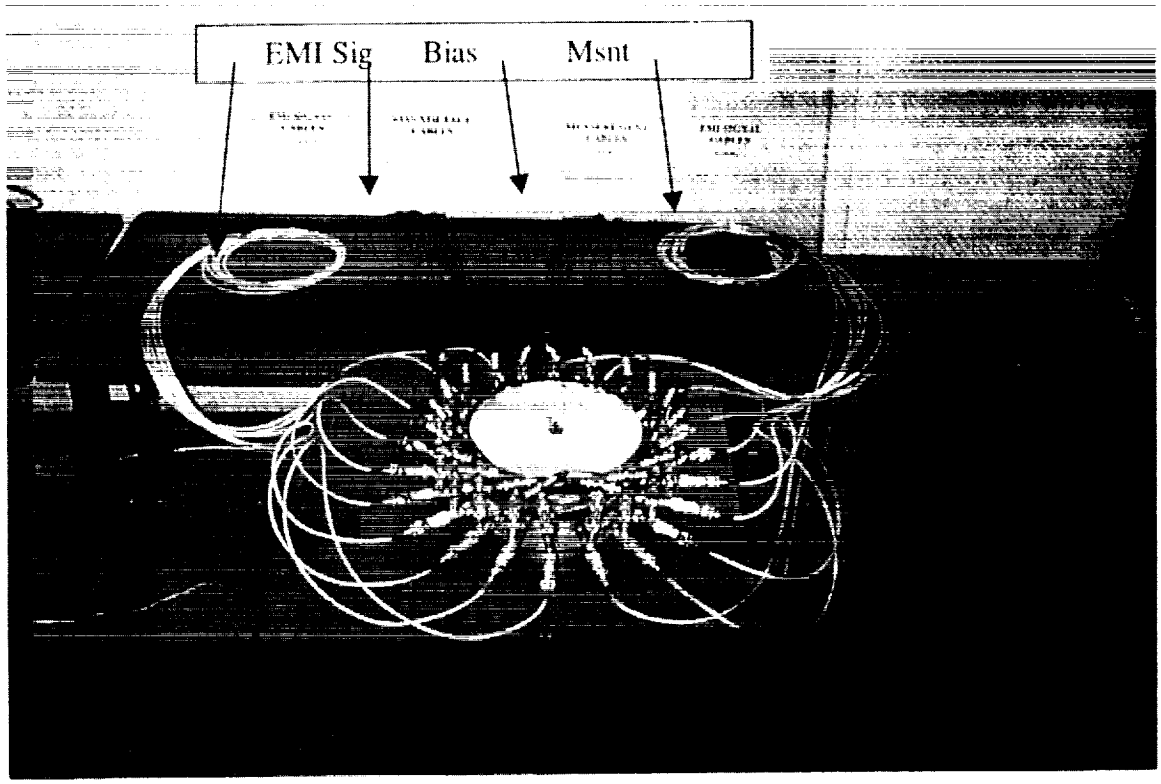


Figure A2- 3. Cabled Test Fixture

A2.4 Summary of Test Process

A much more detailed description is provided in User's manual. A brief overview is provided herein. An IC is initially set up for testing using the Pin Configuration Utility software. A number of test sequences may be generated, depending on the requirements of the device under test. This screen, shown in Figure A2-4, provides for inputs including filename, component nomenclature, number of pins of device being tested, identification of pins for Vcc and ground, designation of a pin to be monitored during the test, a text description of the particular sequence, and assignment of specific parameters to each pin on the chip.

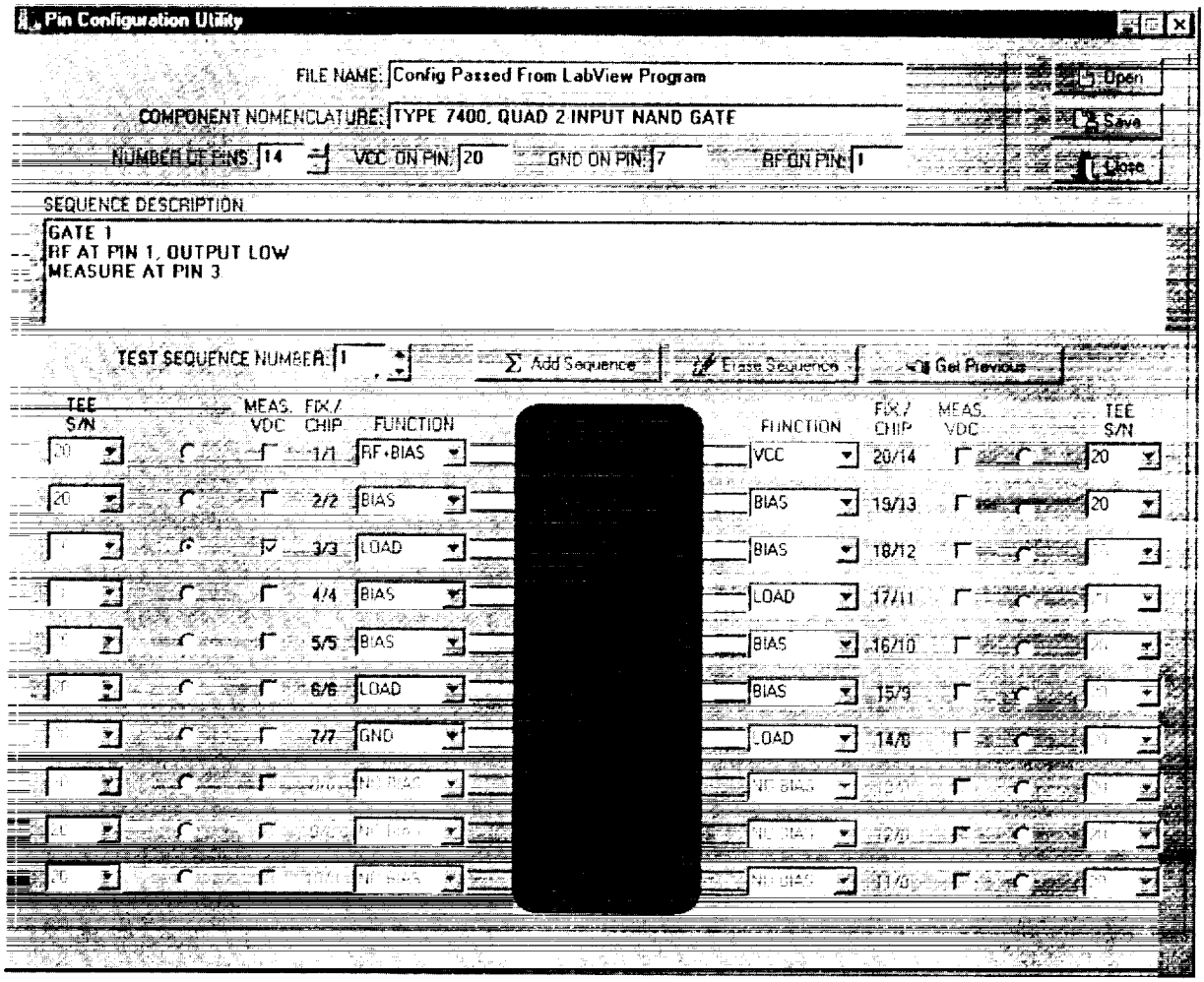


Figure A2- 4. Pin Configuration Utility Screen

These parameter choices are RF, Bias, RF +Bias, Load, RF +Load, Vcc, Ground or No Bias (gnd). The assignment of pins to be measured and/or monitored is also made with this screen. The "MEAS VDC" column designates the output to be measured. Adjacent to that column is an unlabeled column of circles which designates which pin is monitor during test by the "INSTANTANEOUS OUTPUTS" block shown in Figure A2-5. In addition, there is a provision to identify the serial number of the Bias Tees for each pin. The calibration of each Bias Tee is previously stored and automatically applied.

To run the test, use the EMI Test program shortcut to load the Main Panel.vi file. From this screen, shown in Figure A2-5, the user may load a previously saved pin configuration file or create a new one. Once a pin configuration file has been generated and stored, it may be recalled and used any time.

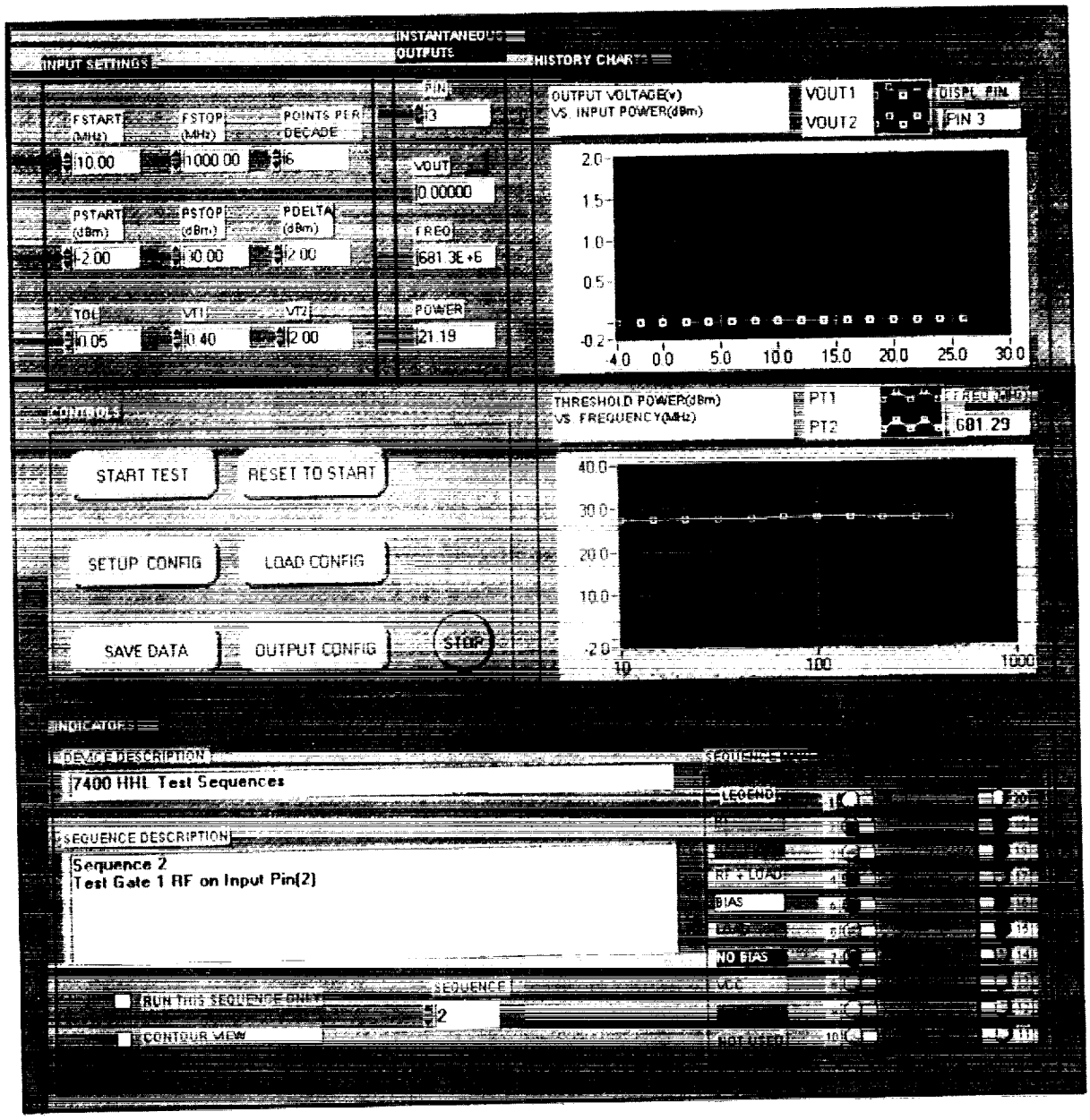


Figure A2- 5. Main Panel.vi Screen

The Main Panel.vi screen has several display blocks. The input settings block selects and displays frequency start and stop points, points per decade, power start and stop points, and power increments to be used. Also shown are the VT1 and VT2 selected voltage threshold indicators.

The controls block has buttons to start test, reset to start, setup pin configuration, load a previously saved configuration, save measured data and select saved data parameters. There is also a STOP button.

The HISTORY CHARTS block graphs near real time data measurements on pins selected on the instantaneous OUTPUTS block. It graphs output voltage vs. input power for the selected pin and immunity level power vs. frequency.

The instantaneous outputs block selects and displays the pin, which is to be measured and displayed. It includes digital displays of voltage, frequency, and power values.

The SEQUENCE MAP displays the selected condition (RF, RF+Bias, Bias, Gnd, or No Bias) for all IC pins under test for a given selected sequence.

A3. Test Process and Results

Integrated circuit (IC) processing for ICE-II involves classification, testing, data merging, and reporting. Classification is the means by which we track a specific IC. A serial number (SN) is assigned to each IC of a study. This SN then becomes the key field on which the relational data base(s) are built.

The ICs are tested in a setup similar to the 7400 NAND gates of Figure A3-1. An EMI signal is injected into a pin of a particular gate while that gate's output voltage level is monitored. A recording is made when the output of the gate under test meets the threshold voltage. Threshold levels are defined as the levels at which the gate-under-test misleads the following circuit into a misinterpretation of the true state of affairs. In Figure A3-1 the EMI signal is applied to a NAND gate input (pin #2) and the gate's output voltage (pin #3) is monitored. If both inputs are High, the NAND gate's output will be Low, i.e., typically less than 0.4 volts for TTL. At a fixed frequency the EMI signal amplitude is slowly increased until the gate's output equals the first threshold, typically 0.8 volts. Between 0.8 and 2.0 volts misinterpretation is possible. The EMI signal's amplitude is increased until the gate's output reaches the second threshold which is where the gate will be misinterpreted, i.e., 2.0 volts, as a High.

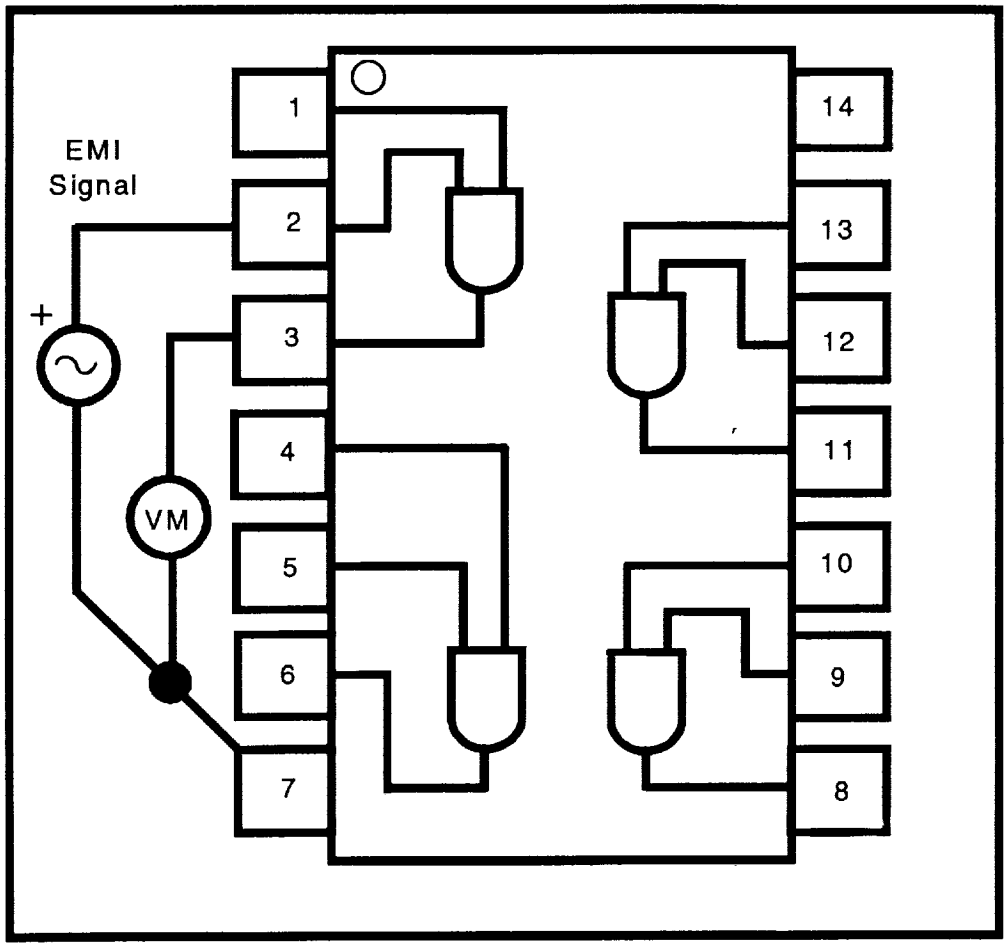


Figure A3- 1. Basic IC Test

An IC study would begin by identifying the classification parameters to be investigated. For example, in the test methodology herein several sets of TTL ICs were identified: totem pole vs. open collector outputs, base TTL vs. LS, ALS, etc. Normally, within one study group the Pin Configuration File would be identical, i.e., all 7400s use the same configuration; although, basic, LS, and ALS were included.

The processing of a particular set of IC's is shown in Figure A3-2. The processing of a specific serial number part number IC is outlined in the flow chart of Figure A3-3. The upper frequency limit, F_{up}, is defined as 10 GHz as the bias tee performance degrades rapidly above this frequency. The MDAC study used an upper frequency of 9.1 GHz. Component susceptibility above 10 GHz is not very significant because of the high impedance of connecting wires and this effect increases with frequency.

The low frequency is limited by the capability of the bias tee to isolate the EMI signal and the bias voltages. From the bias tee calibration curves, 10 MHz, Flow, is a reasonable lower limit using the computer to adjust for the calibration of the bias tees. The MDAC study used a low frequency limit of 220 MHz based primarily on the capability of the bias tees.

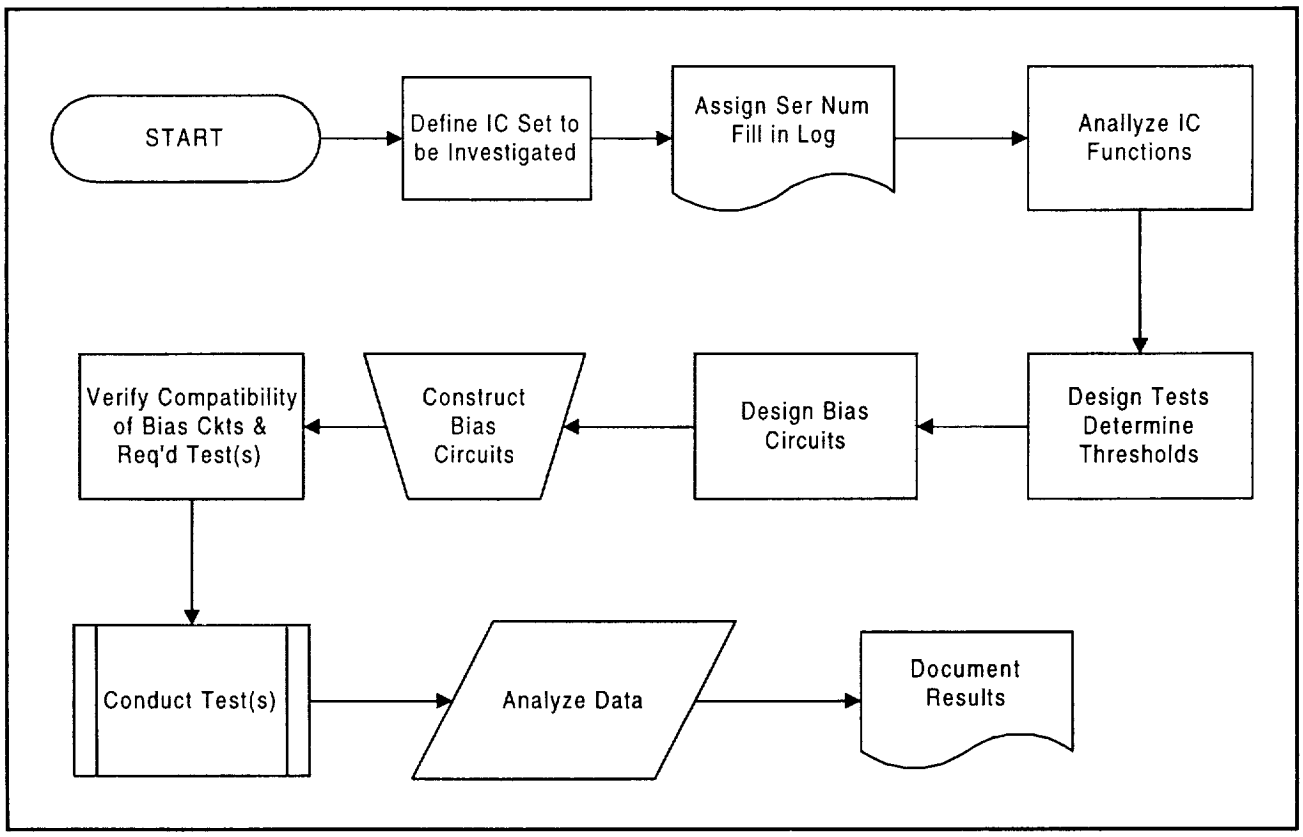


Figure A3- 2. IC Processing Overview

The minimum power level default value was defined as one microwatt, i.e., -30 dBm. The maximum power level was set at one watt, +30 dBm, by equipment limitations. This should be excessive for all but the most resistant IC.

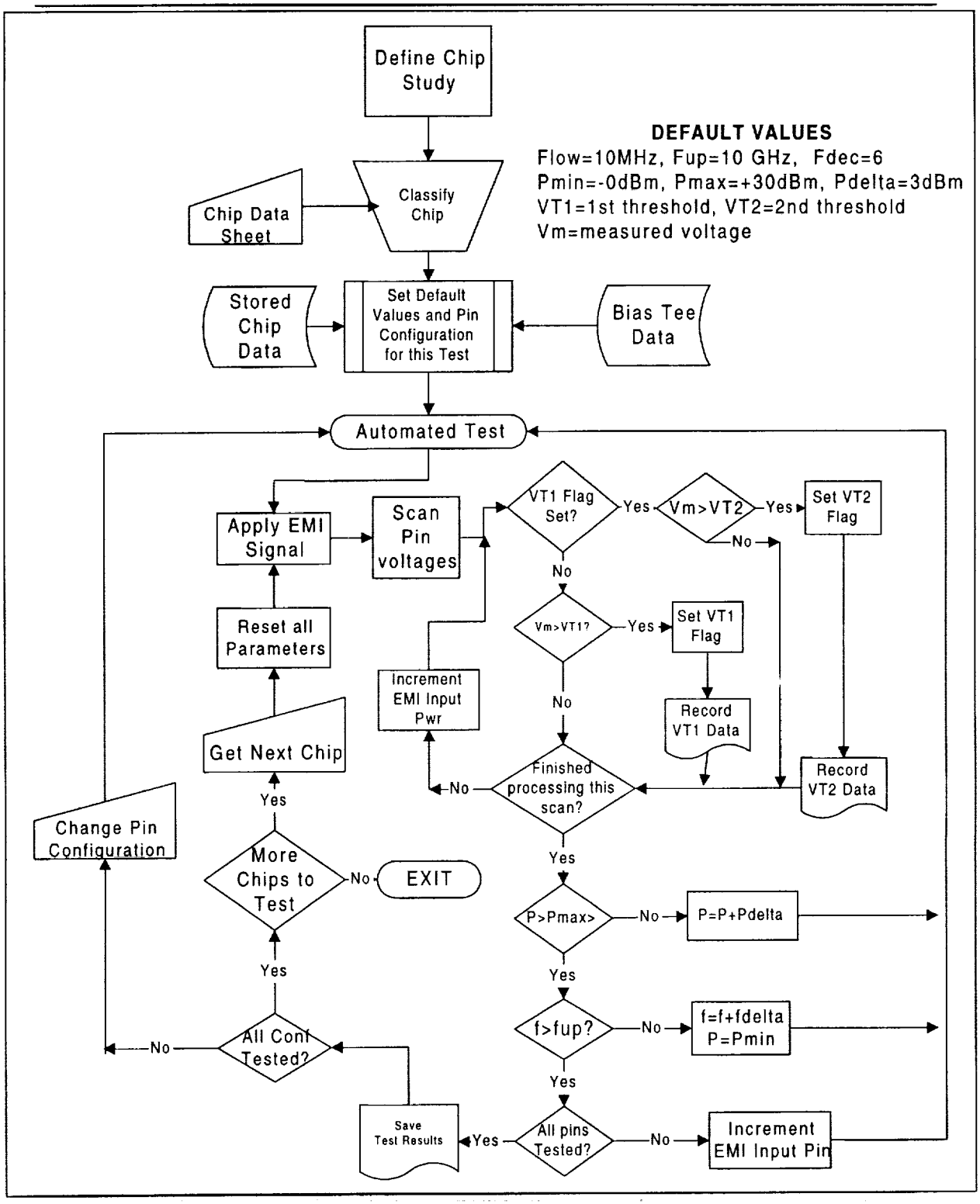


Figure A3- 3. Detailed IC Processing Immunity

A3.1 Thresholds, Validation, and Planning

IC's frequently contain multiple identical circuits within a single IC package, e.g., the 7400 consists of four separate NAND gates all powered via pin 14, Vcc, and pin 7, ground. Therefore, the performance of all four circuits are recorded. There are usually two thresholds, designated V_{T1} and V_{T2}. As the EMI signal is increased, V_{T1} is the first threshold encountered. V_{T2} is the second.

Again using the 7400 as an example, with both inputs High on one of the NAND gates the output will be Low. As the EMI signal is slowly increased in amplitude the output signal will increase. At 0.8 volts the interpretation of the output becomes unreliable (per manufacturer's spec sheet). This is designated V_{T1}. At 2.0 volts the output, per specification, will be interpreted as a High. This is designated as the second threshold, V_{T2}.

Notice the change when one or both inputs are Low, i.e., the output is High (>2.0 volts). A failure is now defined as the output transitions from High to Low. V_{T1}, the first threshold, is 2.0 volts, and V_{T2}, the second threshold, is 0.8 volts.

Software validation was done by testing multiple same PN ICs. There were five of the 7400s and three of the rest. Of course all possible gate configurations and IC configurations were tested.

The EMI Test Plan is a listing of the various test criterion. A copy is contained in the appendix.

A3.2. Test Results

Charts A1 through A11 below depict the immunity of the TTL-type chips tested in this study along with the TTL test results from the work in the seventies. The seventies work included damage assessment, and burnout was expected. Their setup included an RF amplifier to burnout the IC under test. The nineties effort did NOT include burnout as an expected result. The EMI signal was generated by a calibrated source limited to +30 dBm (one watt). With the bias tee and line losses the equipment limitation was about 27 dBm. Consequently the Chart A1-A10 near level plots at 27 dBm represent equipment limitations, not thresholds.

The nineties data plots depict the immunity level to the first threshold by a solid line and the second threshold by a dashed line. On this TTL data from a starting Low (<0.4 volts) the first threshold was 0.8 volts output (below which the following circuit would interpret as a Low), and the second threshold was 2.0 volts (above which the following circuit would interpret as a High). In between (i.e., 0.8 to 2.0 volts) is undefined. Should the particular configuration under test begin with a High (>2.5 volts) the first threshold was

2.0 volts and the second was 0.8 volts. These threshold values were taken from the part manufacturer's specifications.

The seventies criteria were similar, but data detail was limited to what could be extracted from plots in the ICES manual. Also in the seventies data there was no distinction made between types of chips, such as, 7400, 74LS00, 7408, etc., if indeed, there were such differences in the seventies. A quick examination of the charts indicate the seventies data, particularly in frequency, is much more limited than the nineties data. As noted earlier the test frequencies were limited to 220, 910, 3000, 5600, and 9100 MHz. The seventies data was plotted to only 3.0 GHz because there was no susceptibilities within equipment limitations above 3.0 GHz. The nineties data was taken at 6 frequencies per decade, and the graphs were sufficiently close that a smooth curve could be drawn.

Examination of Charts A1 through A10 of Figure A3-4 indicates the nineties ICs are more immune than the seventies ICs were. This should be approached with caution because the nineties data to date does not include a cross-section of manufacturers or date-codes both of which have been found to impact the immunity capability. In general the immune level of TTL type devices appears to exceed 10 dBm for totem-pole devices. This compares favorably with 0 dBm experienced on the seventies project. The open collector devices, 7405 and 74LS05, are slightly less immune than their totem pole counterparts. Again caution is urged until a database has been built to include at least five of each IC.

Chart A1. EMI IMMUNITY LEVEL
7400 NAND GATES

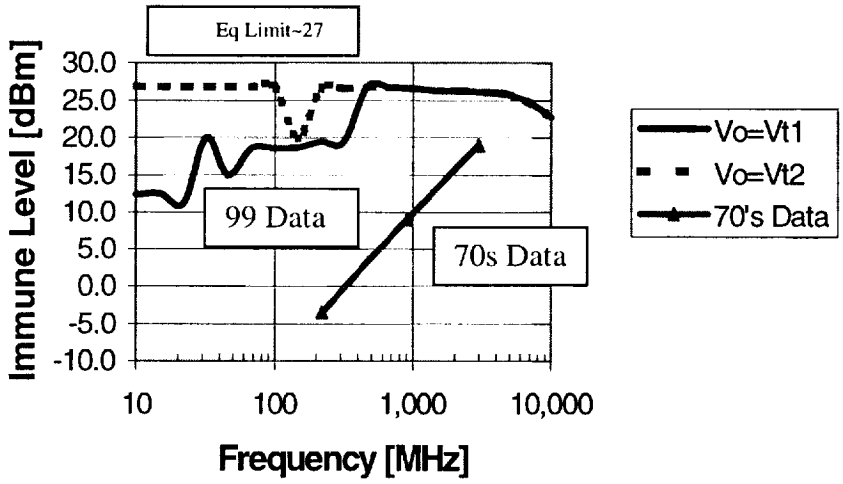


Chart A2. EMI IMMUNITY LEVEL
74ALS00 NAND GATES

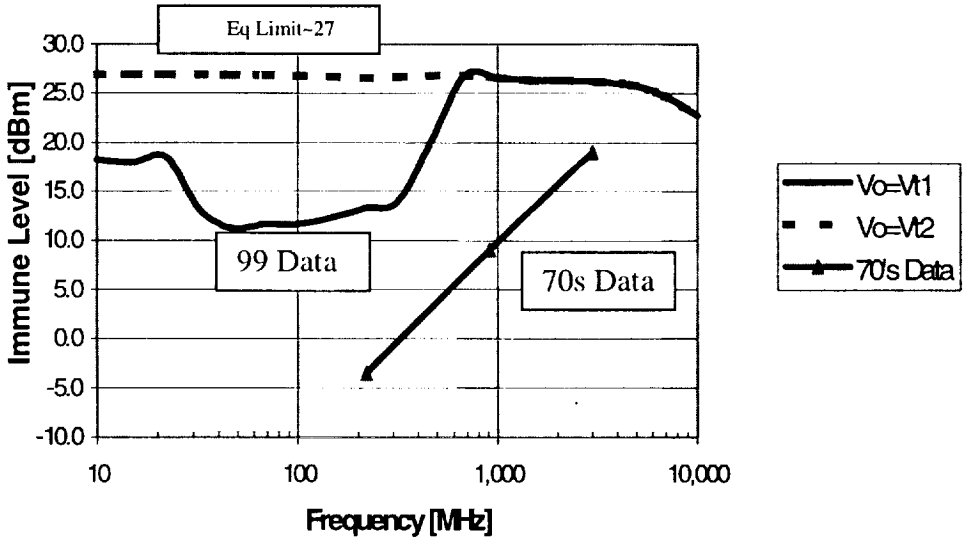


CHART A3. EMI IMMUNITY LEVEL 74LS00 NAND GATES

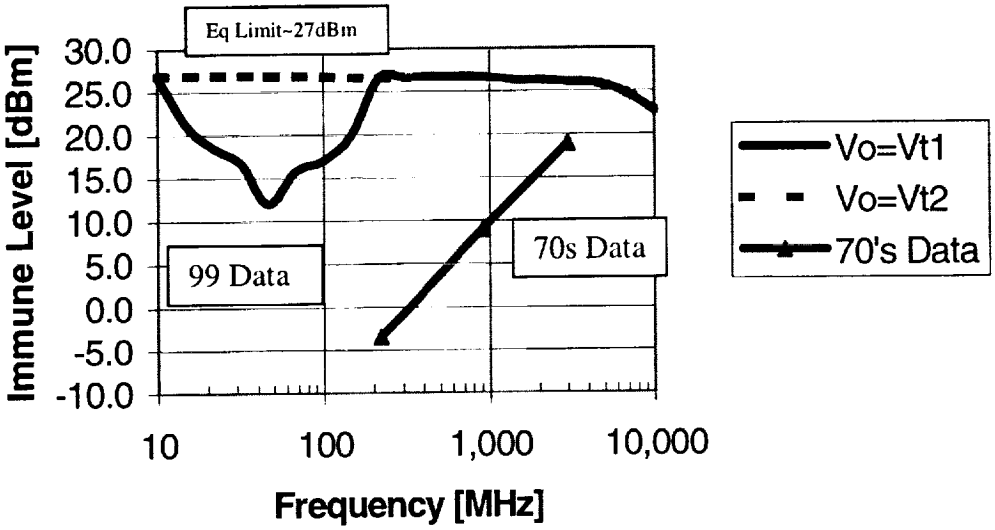
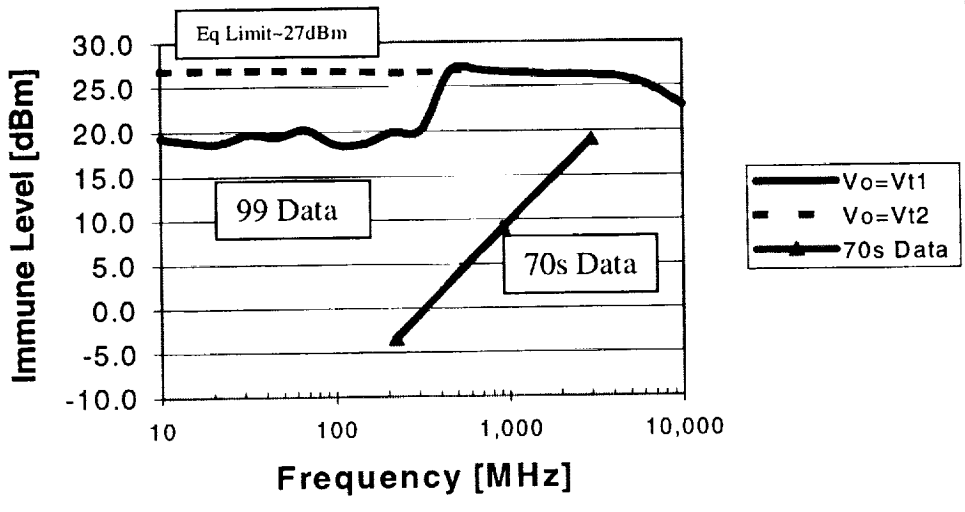


Chart A4. EMI IMMUNITY LEVEL 7408 AND GATES



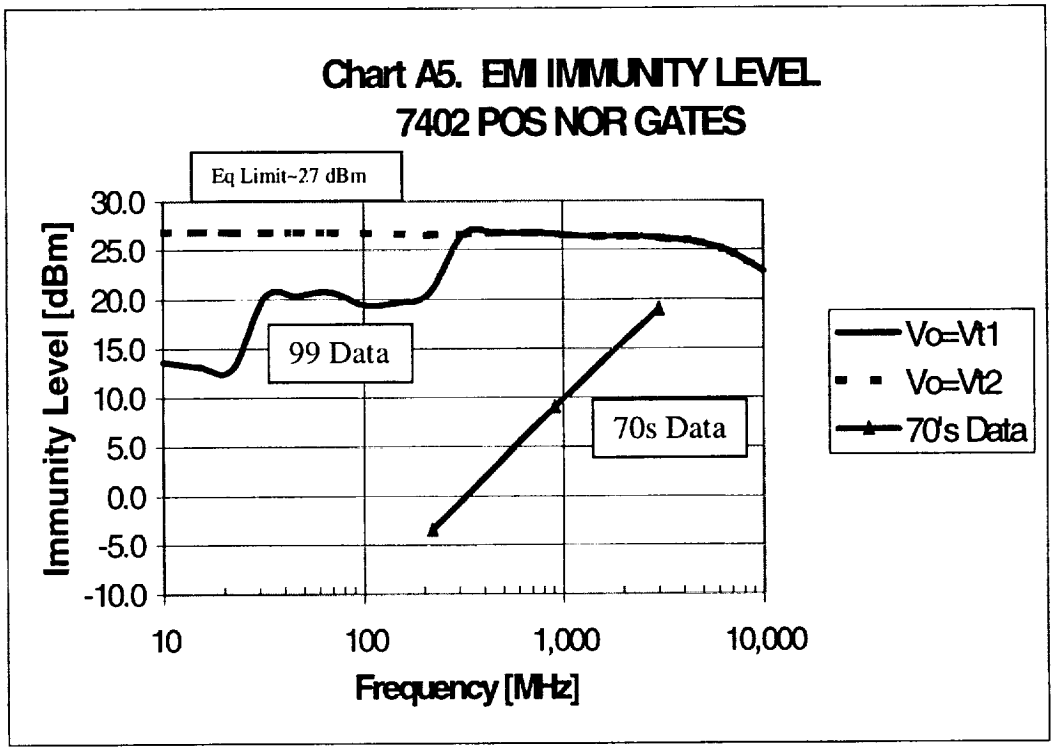


Chart A5. EMI IMMUNITY LEVEL
7402 POS NOR GATES
Eq Limit-27 dBm
99 Data
70s Data
Immunity Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

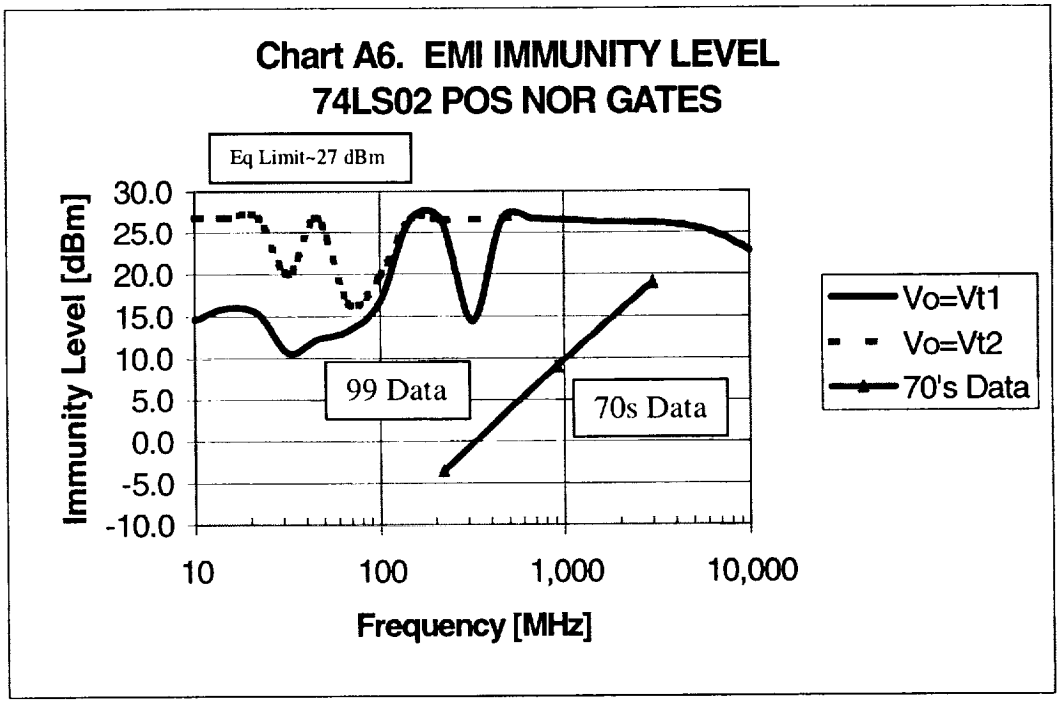


Chart A6. EMI IMMUNITY LEVEL
74LS02 POS NOR GATES
Eq Limit-27 dBm
99 Data
70s Data
Immunity Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

Chart A7. EMI IMMUNITY LEVEL 7404 TOTEM POLE INVERTER

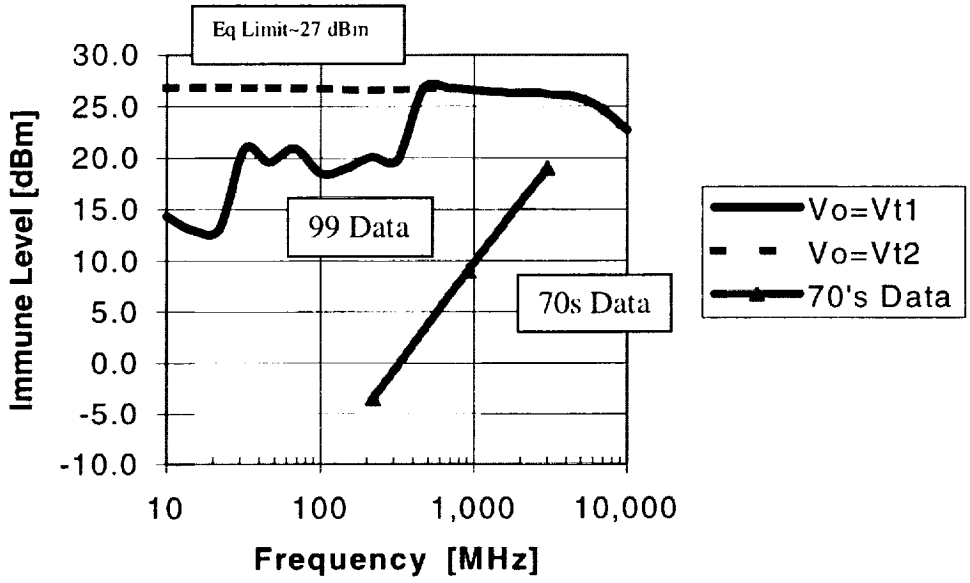
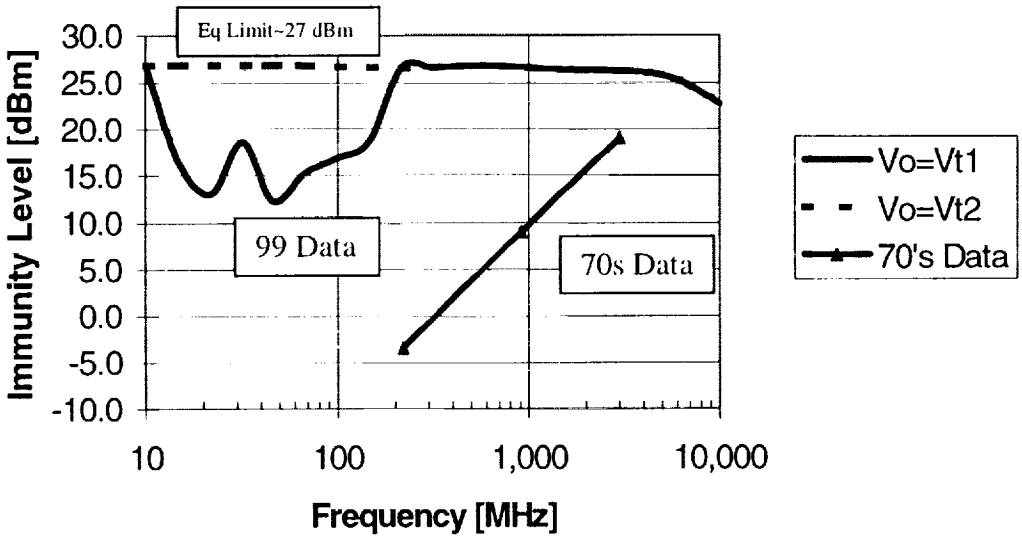


Chart A8. EMI IMMUNITY LEVEL 74LS04 TOTEM POLE INVERTER



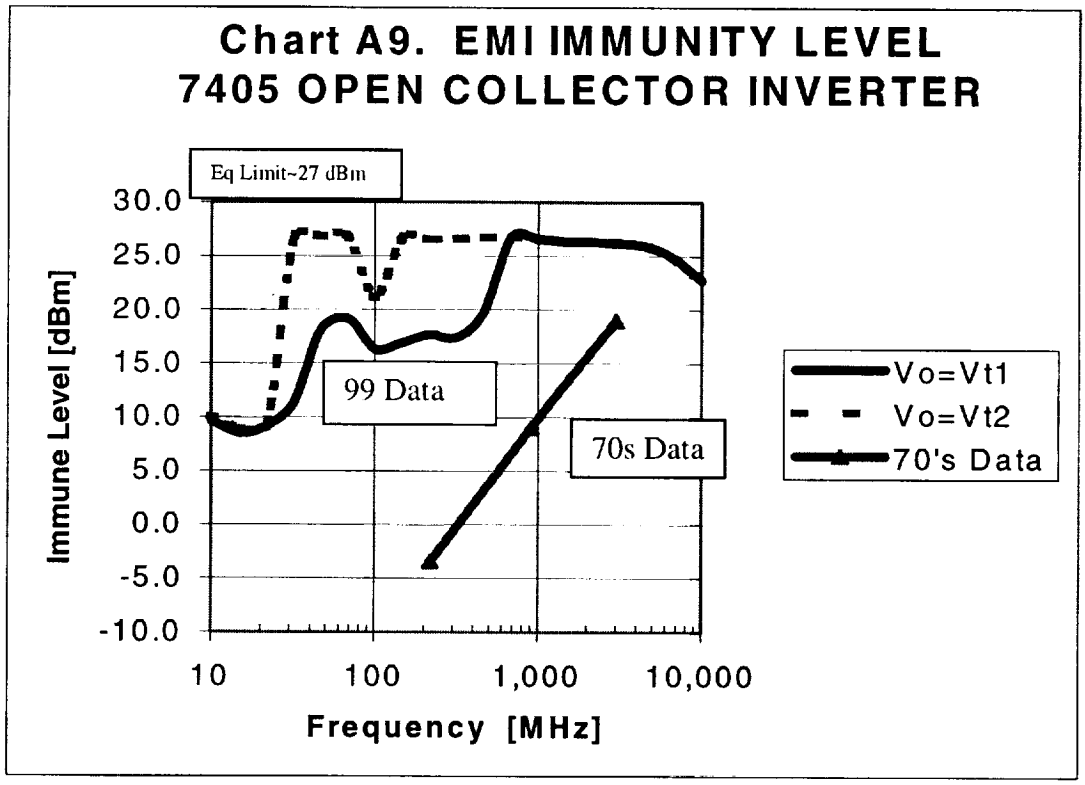


Chart A9. EMI IMMUNITY LEVEL
7405 OPEN COLLECTOR INVERTER
Eq Limit~27 dBm
99 Data
70s Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

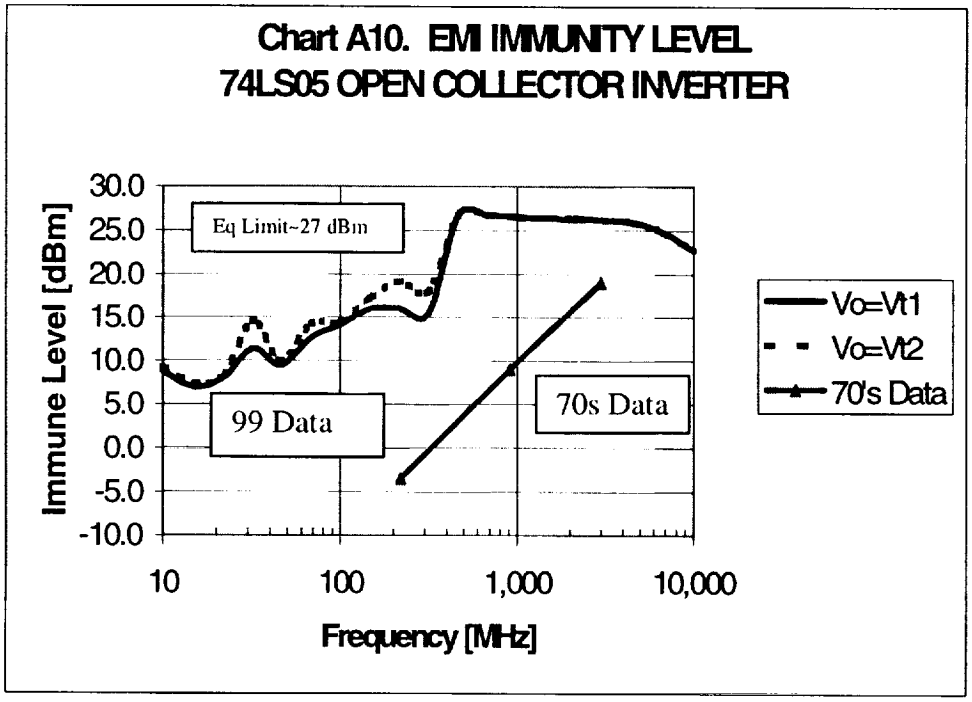


Chart A10. EMI IMMUNITY LEVEL
74LS05 OPEN COLLECTOR INVERTER
Eq Limit~27 dBm
99 Data
70s Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

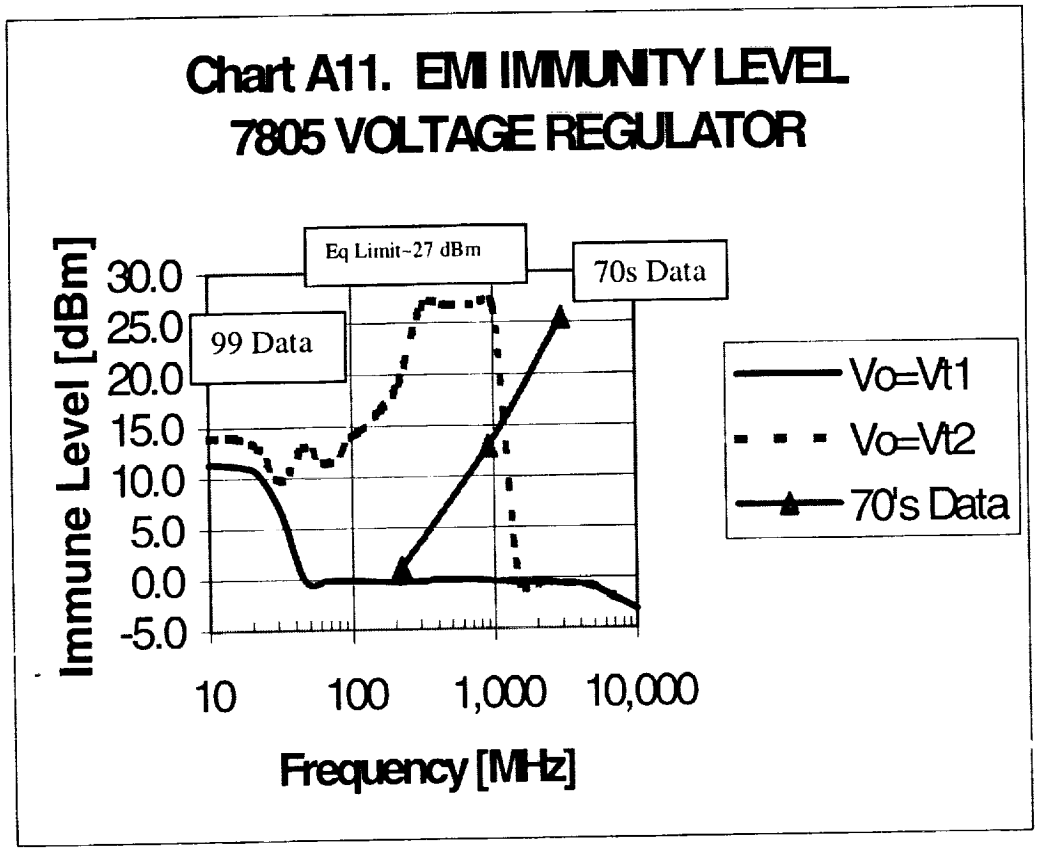


Chart A11. EMI IMMUNITY LEVEL
7805 VOLTAGE REGULATOR
Eq Limit-27 dBm
70s Data
99 Data
Immune Level [dBm]
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
10
100
1,000
10,000
Frequency [MHz]
Vo=Vt1
Vo=Vt2
70's Data

References

1. Integrated Circuit Electromagnetic Susceptibility Handbook, McDonnell Douglas Corporation Report MDC E1929, 1 August 1978

2. Report No. D950-10465-1 — Integrated Circuit Electromagnetic Immunity, Volume 1 — Final Report, 31 December 1999

3. Report No. D950-10465-2 — Integrated Circuit Electromagnetic Immunity Volume 2 — Handbook, 31 December 1999

4. Report No. D950-10466-1 — Integrated Circuit Electromagnetic Immunity User's Manual, 31 December 1999

Appendix A: EMI Test Plan

Type Chip	Chip SN	Descr	Test Conf In In Out	Start Freq	Stop Freq	Threshold #1	Threshold #2
DN7400N	0001	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0001	2-INPUT	LHH			2.0	0.8
	0001	NAND	HLH			2.0	0.8
	0001	GATES	LLH			2.0	0.8
	0002	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0002	2-INPUT	LHH			2.0	0.8
	0002	NAND	HLH			2.0	0.8
	0002	GATES	LLH			2.0	0.8
	0003	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0003	2-INPUT	LHH			2.0	0.8
	0003	NAND	HLH			2.0	0.8
	0003	GATES	LLH			2.0	0.8
	0004	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0004	2-INPUT	LHH			2.0	0.8
	0004	NAND	HLH			2.0	0.8
	0004	GATES	LLH			2.0	0.8
DM74ALS00AN	0005	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0005	2-INPUT	LHH			2.0	0.8
	0005	NAND	HLH			2.0	0.8
	0005	GATES	LLH			2.0	0.8
	0006	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0006	2-INPUT	LHH			2.0	0.8
	0006	NAND	HLH			2.0	0.8
	0006	GATES	LLH			2.0	0.8
	0007	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0007	2-INPUT	LHH			2.0	0.8
	0007	NAND	HLH			2.0	0.8
	0007	GATES	LLH			2.0	0.8

Type Chip	Chip SN	Descr	Test Conf In In Out	Start Freq	Stop Freq	Threshold #1	Threshold #2
DM74LS00N-ND	0008	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0008	2-INPUT	LHH			2.0	0.8
	0008	NAND	HLH			2.0	0.8
	0008	GATES	LLH			2.0	0.8
	0009	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0009	2-INPUT	LHH			2.0	0.8
	0009	NAND	HLH			2.0	0.8
	0009	GATES	LLH			2.0	0.8
	0010	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
	0010	2-INPUT	LHH			2.0	0.8
	0010	NAND	HLL			2.0	0.8
	0010	GATES	LLH			2.0	0.8
DM7402N	0011	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
		2-INPUT	LHL			0.8	2.0
		POS	HLL			0.8	2.0
		NOR	LLH			2.0	0.8
	0012	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
		2-INPUT	LHL			0.8	2.0
		POS	HLL			0.8	2.0
		NOR	LLH			2.0	0.8
	0013	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
		2-INPUT	LHL			0.8	2.0
		POS	HLL			0.8	2.0
		NOR	LLH			2.0	0.8
DM74LS02N-ND	0014	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
		2-INPUT	LHL			0.8	2.0
		POS	HLL			0.8	2.0
		NOR	LLH			2.0	0.8
	0015	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
		2-INPUT	LHL			0.8	2.0
		POS	HLL			0.8	2.0
		NOR	LLH			2.0	0.8

Type Chip	Chip SN	Descr	Test Conf In In Out	Start Freq	Stop Freq	Threshold #1	Threshold #2
DM74LS02N-ND	0016	QUAD	HHL	10 MHz	10 GHz	0.8	2.0
		2-INPUT	LHL			0.8	2.0
		POS	HLL			0.8	2.0
		NOR	LLH			2.0	0.8
DM7404N	0017	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		TOTEM	LH			2.0	0.8
	0018	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		TOTEM	LH			2.0	0.8
	0019	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		TOTEM	LH			2.0	0.8
DM74LS04N-ND	0020	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		TOTEM	LH			2.0	0.8
	0021	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		TOTEM	LH			2.0	0.8
	0022	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		TOTEM	LH			2.0	0.8
DM7405N	0023	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		O.C.	LH			2.0	0.8
	0024	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		O.C.	LH			2.0	0.8
	0025	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		O.C.	LH			2.0	0.8
DM74LS05N-ND	0026	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		O.C.	LH			2.0	0.8
	0027	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		O.C.	LH			2.0	0.8
	0028	HEX INV	HL	10 MHz	10 GHz	0.8	2.0
		O.C.	LH			2.0	0.8

Type Chip	Chip SN	Descr	Test Conf In In Out	Start Freq	Stop Freq	Threshold #1	Threshold #2
DM7408N	0029	QUAD	HHH	10 MHz	10 GHz	2.0	0.8
		2-INPUT	LHL			0.8	2.0
		AND	HLL			0.8	2.0
		GATES	LLL			0.8	2.0
	0030	QUAD	HHH	10 MHz	10 GHz	2.0	0.8
		2-INPUT	LHL			0.8	2.0
		AND	HLL			0.8	2.0
		GATES	LLL			0.8	2.0
	0031	QUAD	HHH	10 MHz	10 GHz	2.0	0.8
		2-INPUT	LHL			0.8	2.0
		AND	HLL			0.8	2.0
		GATES	LLL			0.8	2.0
LINEAR							
LM309K STEEL	A0001						
	A0002						
	A0003						
LM339NNS	A0004						
	A0005						
	A0006						
LM78L05ACH-ND	A0007						
	A0008						
	A0009						

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13. ABSTRACT *(Maximum 200 words)*

This handbook presents the results of the Boeing Company effort for NASA under contract NAS8–98217. Immunity level data for certain integrated circuit parts are discussed herein, along with analytical techniques for applying the data to electronics systems. This handbook is built heavily on the one produced in the seventies by McDonnell Douglas Astronautics Company (MDAC, MDC Report E1929 of 1 August 1978, entitled Integrated Circuit Electromagnetic Susceptibility Handbook, known commonly as the ICES Handbook, which has served countless systems designers for over 20 years).

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